Forum *Romanians in Micro- and Nanoelectronics,* *6 November 2018, Romanian Academy, Bucharest, Romania*

Engineered Substrates and Technologies for Nanoelectronics

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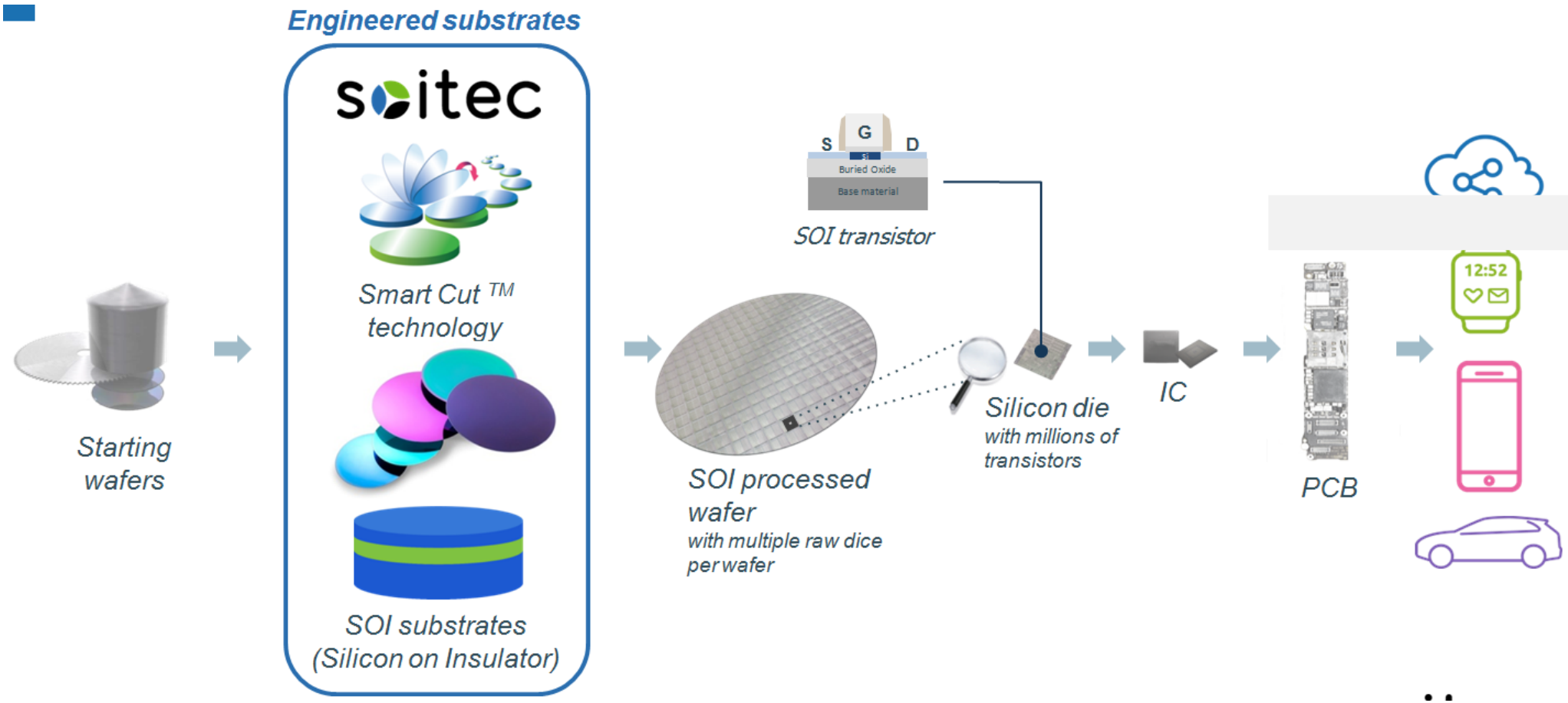
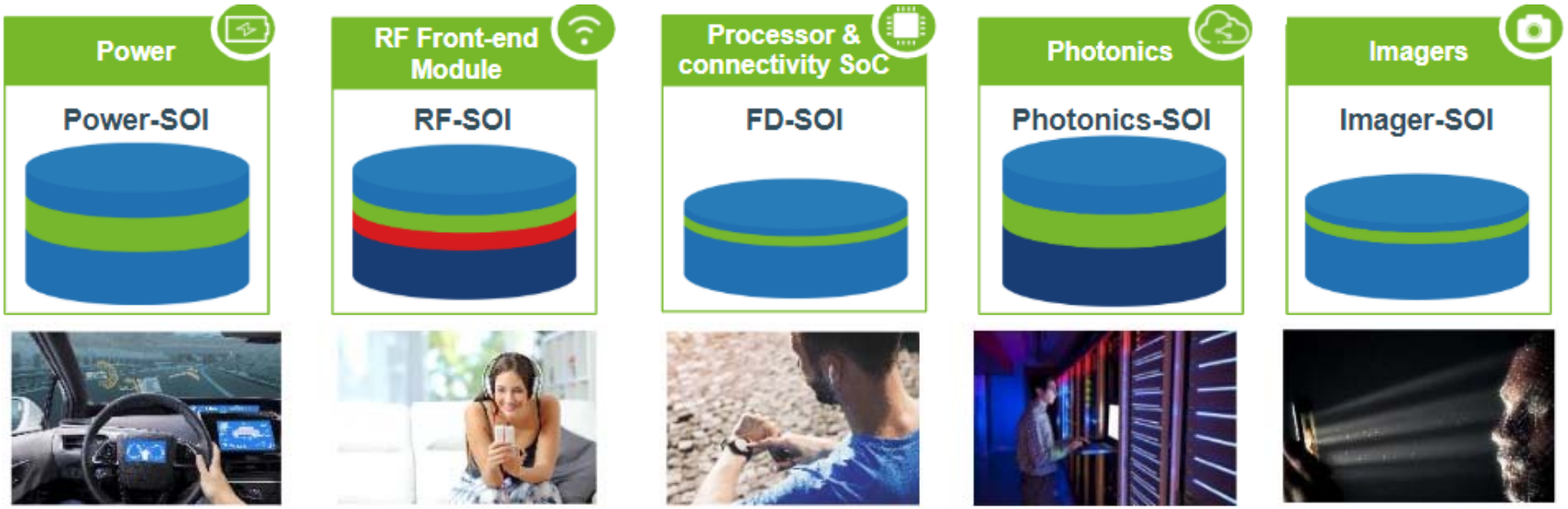
Semiconductor Value Chain



Leading engineered substrate supplier addressing consumer markets



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OUTLINE

1. Value of substrate engineering
2. Substrate technologies & some physics insights
3. Innovation model
4. Takeaways

~~Challenges~~ Opportunities for semiconductor innovation

SMARTPHONES

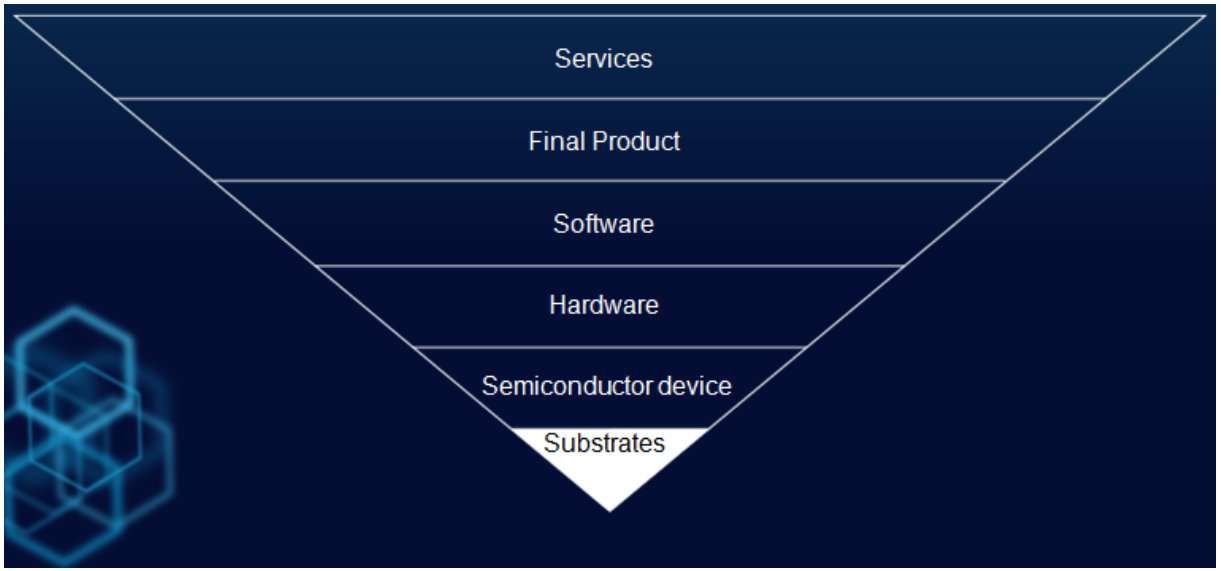
AUTOMOTIVE

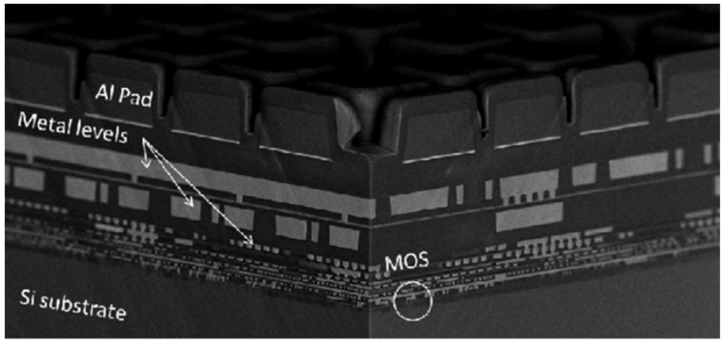
5G

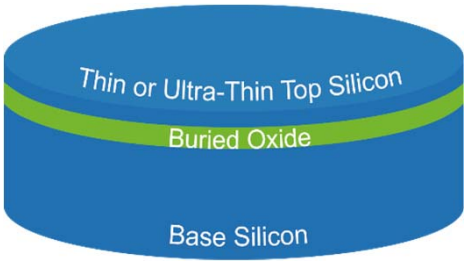
IOT

ARTIFICIAL INTELLIGENCE

Substrates are the foundation of high-tech products

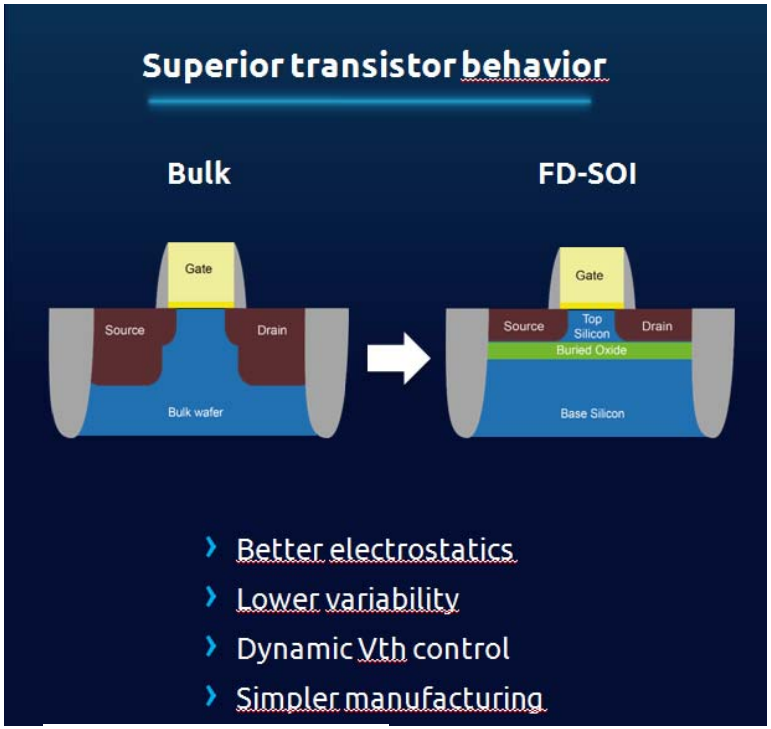


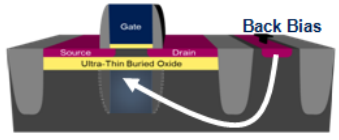




The characteristics of the initial substrate define the performance and architecture of devices and circuits

FD-SOI technology





P. Flatresse et al.
S3S Conference Short Course, 2014

- **Power**
  - Junction capacitance removal
  - Body Bias enabling ULV operation

- **Performance**
  - Sub 20nm device scaling
  - Very low mismatch
  - On demand performance through body bias
  - mmWave compatible RF device
  - Immunity to high energy particules
  - Superior analog device behavior compared to bulk
  - Process, temperature & ageing compensation through body bias

- **Cost**
  - Lower manufacturing cost for foundry than bulk
  - Lower NRE than FinFET

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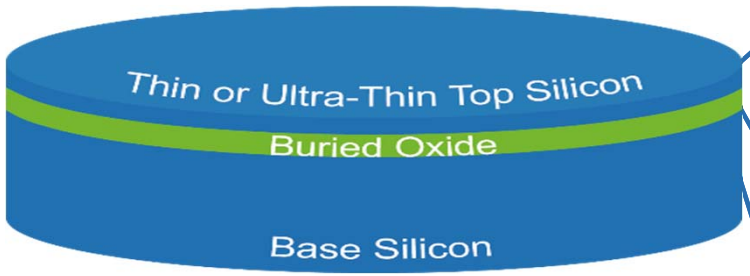
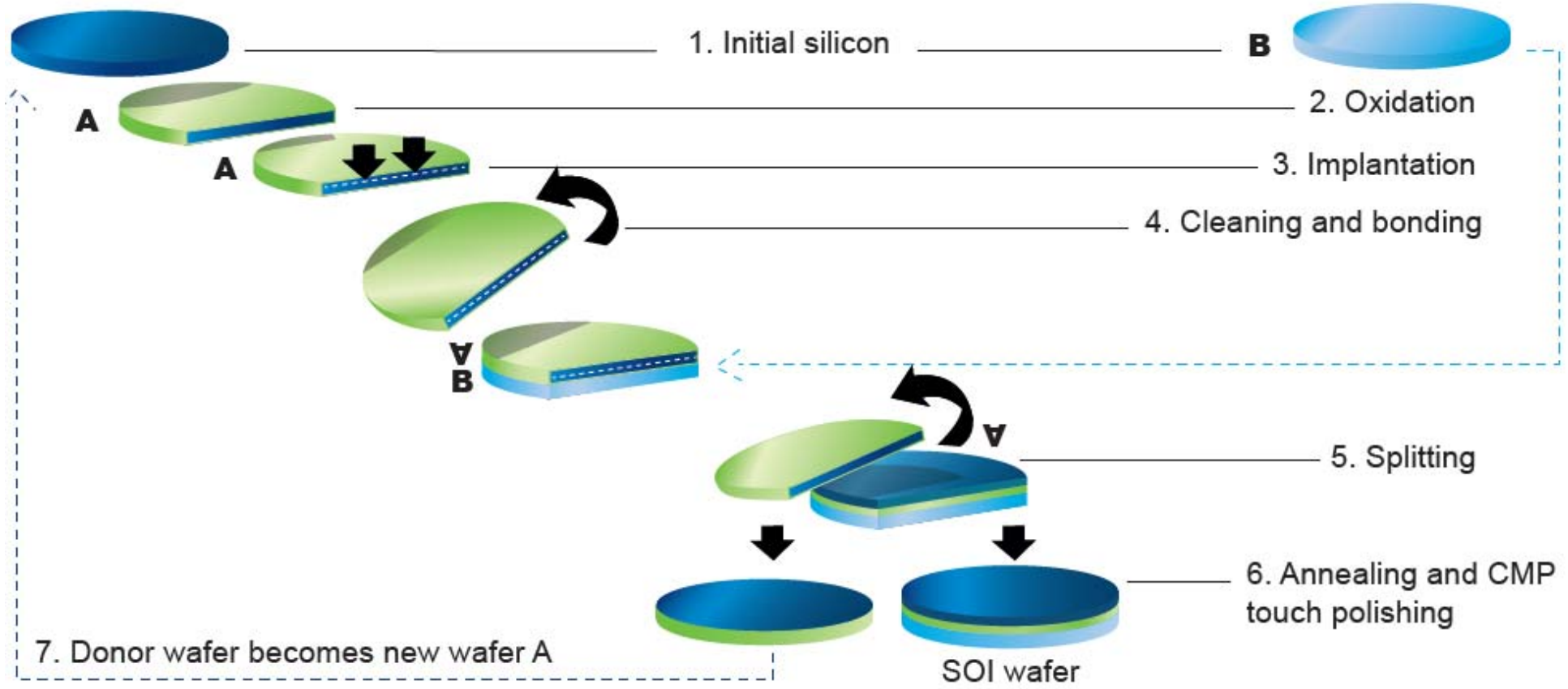
Transistor channel and back-gate oxide @substrate

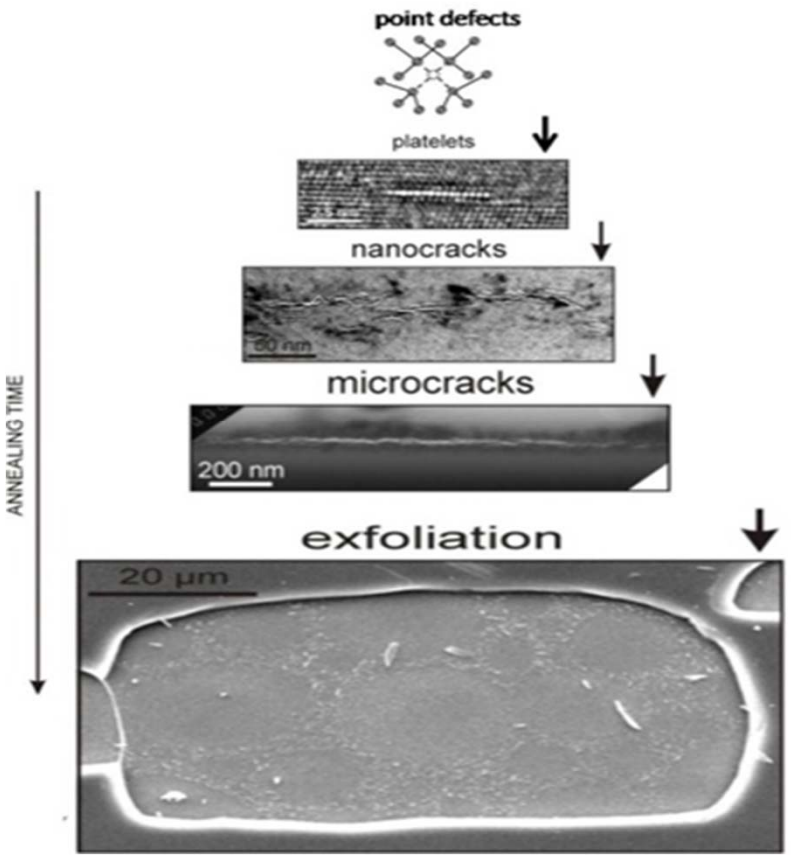


Substrate characteristics	Device benefits
Thickness Uniformity	Electrostatics
Micro-roughness Macro-roughness	Variability
Electrical properties	Mobility
Defectivity Metal contamination	Yield
Thickness Uniformity	Electrostatics Back gate control
Parasitics charges Integrity (Breakdown voltage)	Variability, Reliability
Geometry Bulk Micro Defects Metal contamination	Yield + variability

Smart Cut™ : revolutionary technology



Smart Cut process: multiscale, multiphysics phenomena



Scale

Å

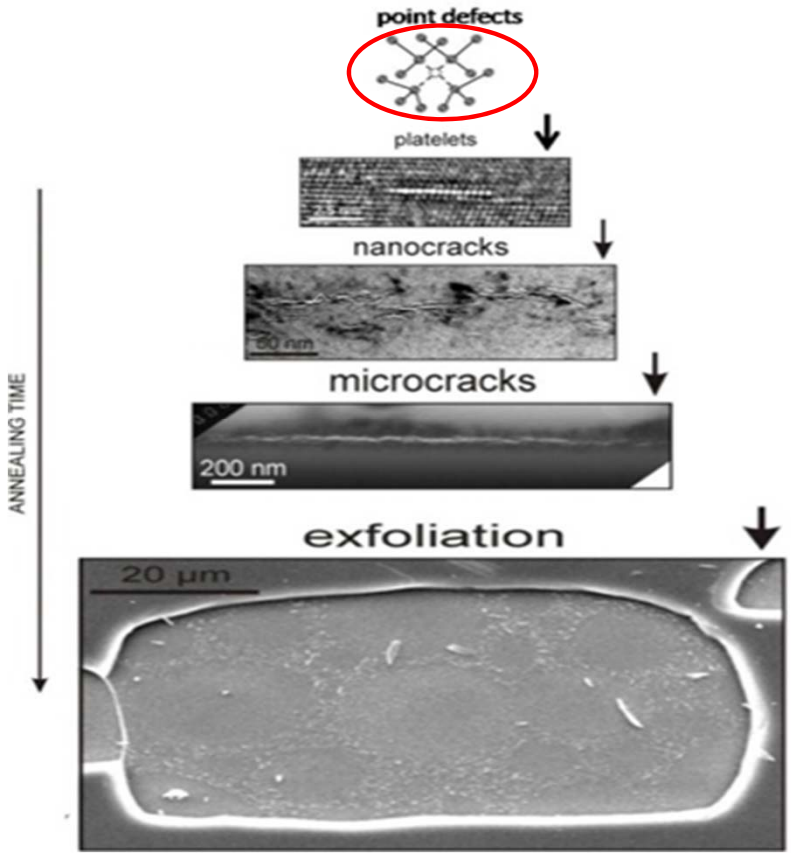
nm

tens of nm

µm

mm

Smart Cut process: multiscale, multiphysics phenomena



Scale

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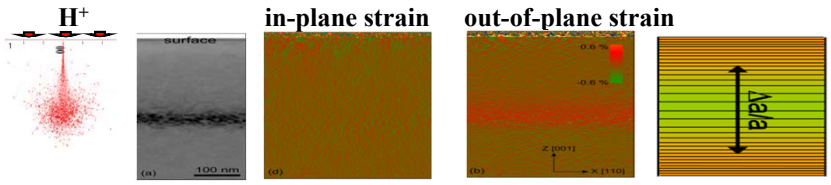
nm

tens of nm

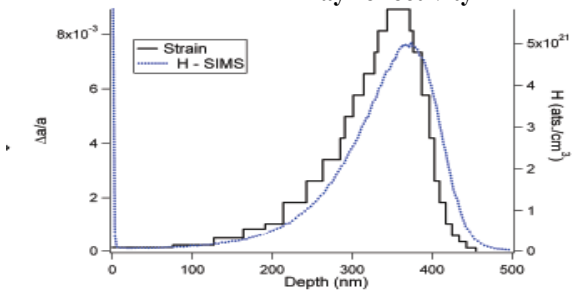
µm

mm

Dark-Field holography



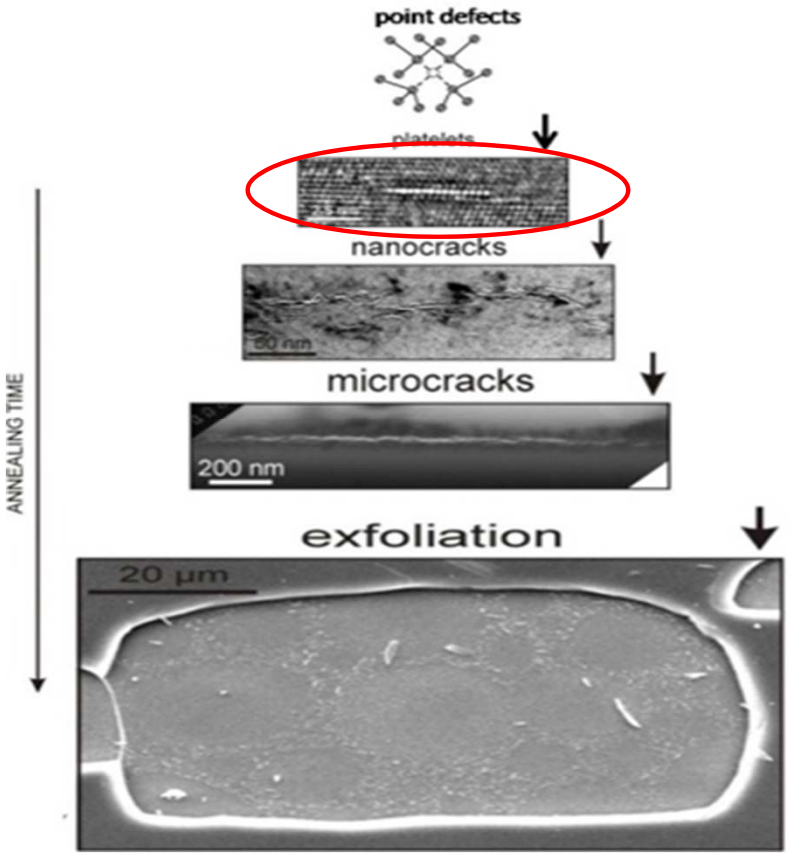
X-Ray reflectivity



See e.g. Sousbie, Capello, JAP(2006)

Generation of point defects and vertical stress

Smart Cut process: multiscale, multiphysics phenomena



Scale

Å

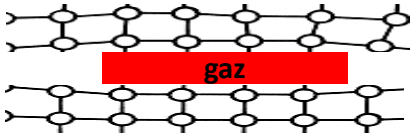
nm

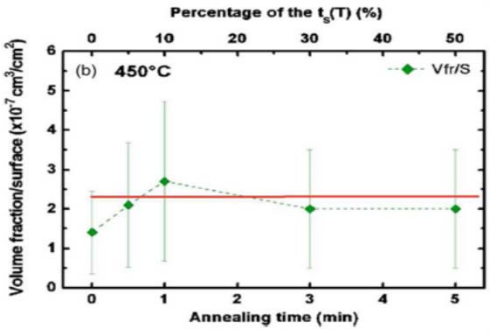
tens of nm

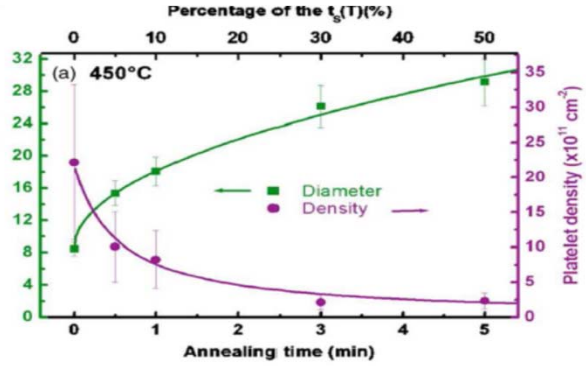
µm

mm

H & Vacancy co-precipitation in Platelets

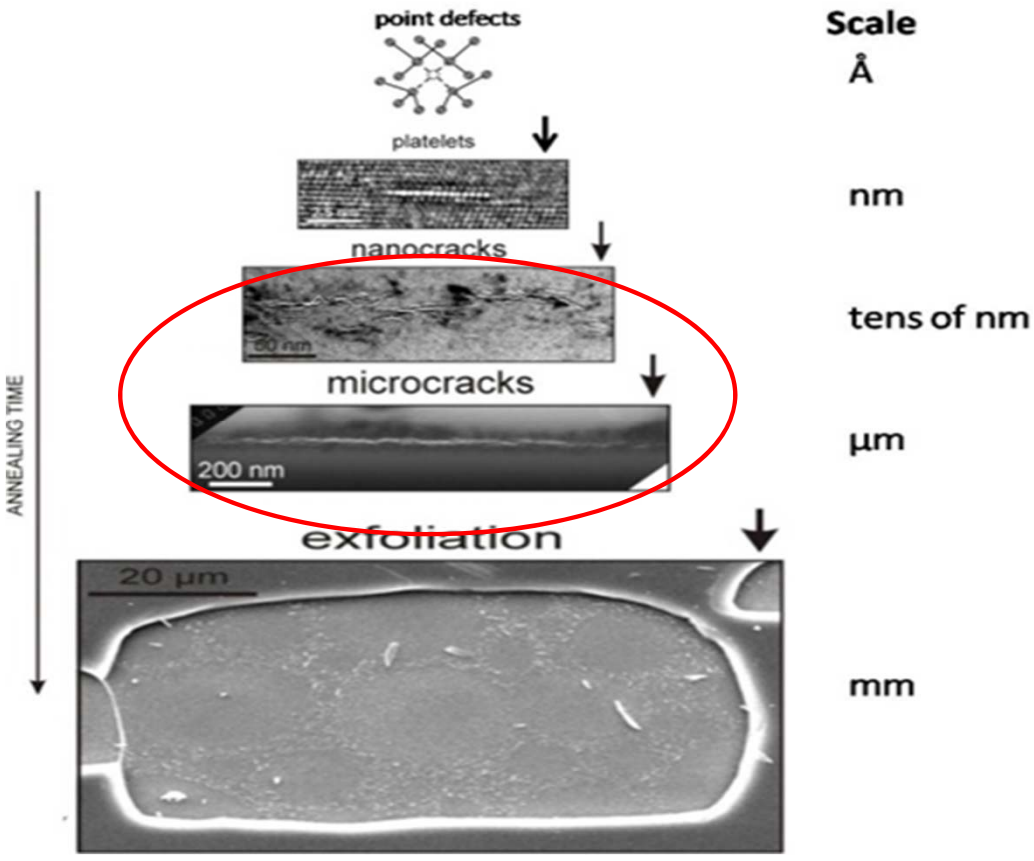






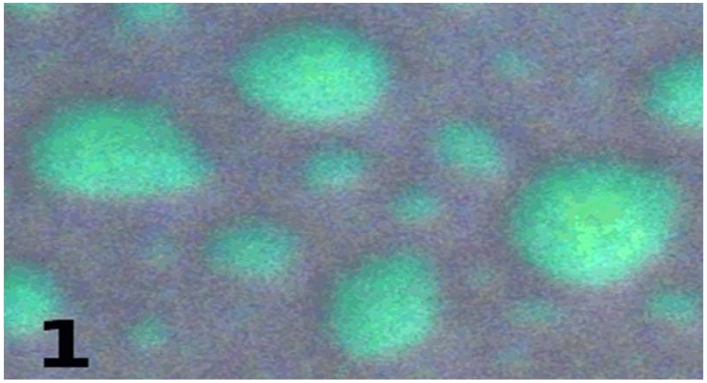
Platelets growth (Conservative Ostwald ripening)

Smart Cut process: multiscale, multiphysics phenomena

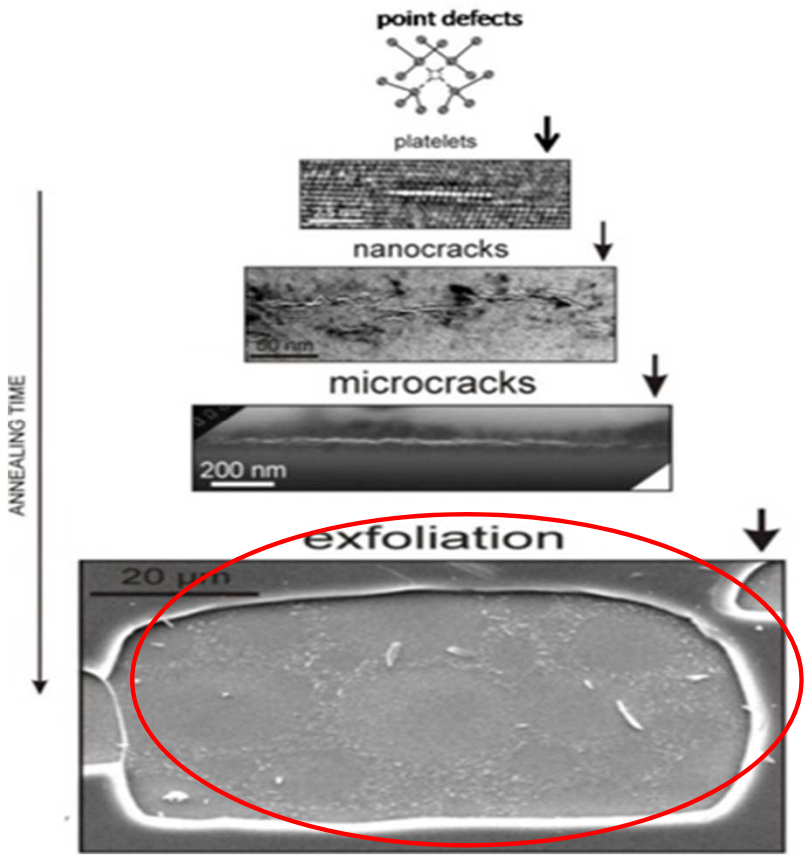


Nanocrack Ostwald ripening study in-situ

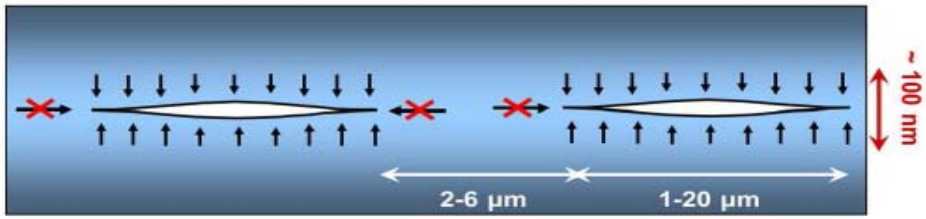
Microcrack coalescence by IR microscopy



Smart Cut process: multiscale, multiphysics phenomena



$$Log(\frac{1}{\tau_{Split}}) = C - \frac{E_a}{k_B T} - \frac{\gamma}{\frac{3}{8}\rho_S \, k_B T} + ... + O(LogT)$$



Minimization of total energy:
Platelets reduction → microcracks growth

Model:
vertical H diffusion from platelets + Griffits criteria

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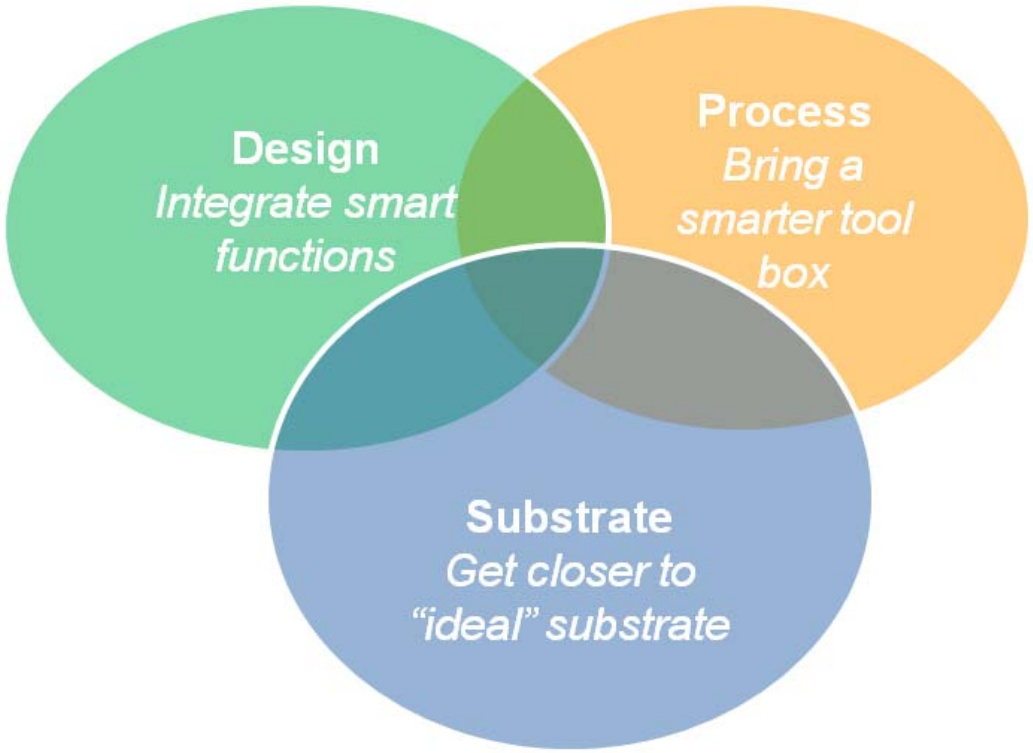
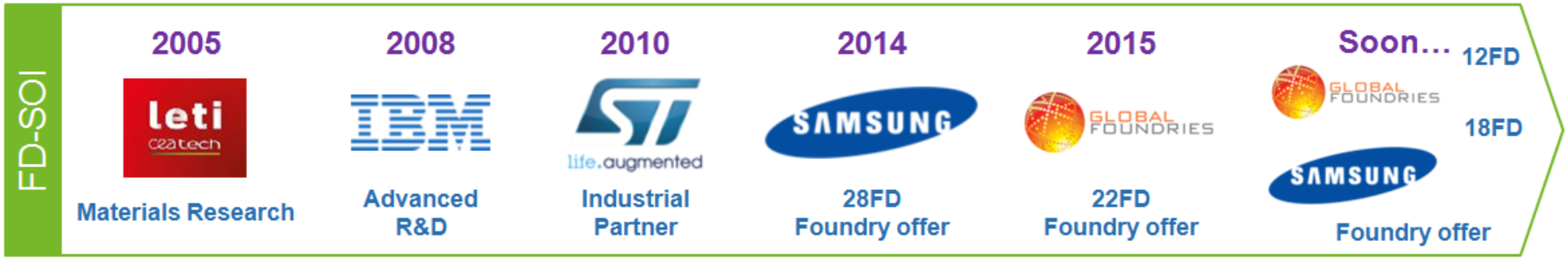
Collaborative R&D – successful innovation model



Complete ecosystem across the value chain working to meet product specifications

SOI adoption through key partnerships and collaborations

RF-SOI & FD-SOI: European leadership in innovation



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Take aways

- Engineered Substrates represent **foundation of advanced electronic circuits**
- Soitec's technology roadmap will continue to enable next generation of devices
- System Design-Technology-Substrate co-optimization is required to establish technology standards: **collaborative R&D**
- Smart Things Opportunity ahead: 5G, AI, Automotive, Health & Medical