Systematic and optimized design of analog ICs

Marius Neag, Technical University, Cluj-Napoca, Romania

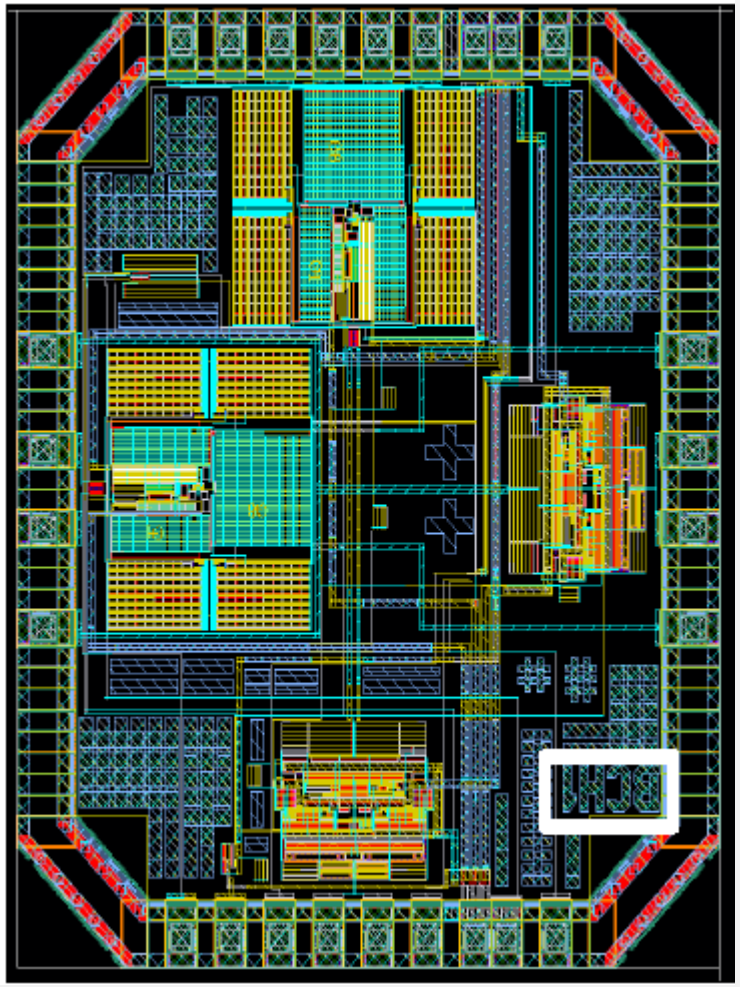
Revised version 06.12.2018

Overview

- *The "DERFAIC"* Research Group
  - Brief description
  - Examples of ICs and modules developed by DERFAIC members
- Systematic and optimized design
  - Main Approaches
  - Design Example: standard OpAmp with Miller Rc-Cc frequency compensation
- Low Drop-Out Voltage Regulators (LDOs) designed by PHD students
  - Main design challenges
  - Error amplifier
    - Larger SR for faster transient response: Class-AB Recycling Folded Cascode OTAs
  - Over-Current Protection
    - Improved design by using Electro-Thermal simulations
  - Over-Temperature Protection
    - Design methodology based on Electro-Thermal simulations
    - Design Example
- Summary and Conclusions

DERFAIC research group: Main areas of activity

- Design of RF, Analog and Mixed–Signal Integrated Circuits (ICs)
- Design and physical implementation of board-level modules with ICs
- Optimization techniques and tools for synthesis of analog and digital circuits
- Modelling and characterization of integrated circuits and systems
- Multifactor analysis of integrated circuits and systems, yield analysis
- High performance power management circuitry, including energy harvesting & conversion and wireless power transfer
- Electronic circuits and systems for acoustics: modelling the acoustic behavior of enclosures, optimized synthesis of acoustic equalizers
- Website: http://icdesign.utcluj.ro



DERFAIC research group: Resources

Staff

- 8 academic staff members
- 10 PhD students
- 5 MSc and BSc students with scholarships

Funding sources

- research grants with public funding
- R&D services for companies within the semiconductor industry

Infrastructure

- 2 laboratories with dedicated computer network
- 2 laboratories with standard equipments

Technical support

- Cadence Academic Network membership
  - Access to state-of-the-art Cadence suites of IC design tools
  - Access to technical support, courses and training sessions
- Europractice membership
  - Access to 90nm, 0.15um and 0.18um CMOS based logic, RF/mixed-signal and high-voltage CMOS technologies
  - Access to state-of-the-art manufacturing facilities for IC prototyping

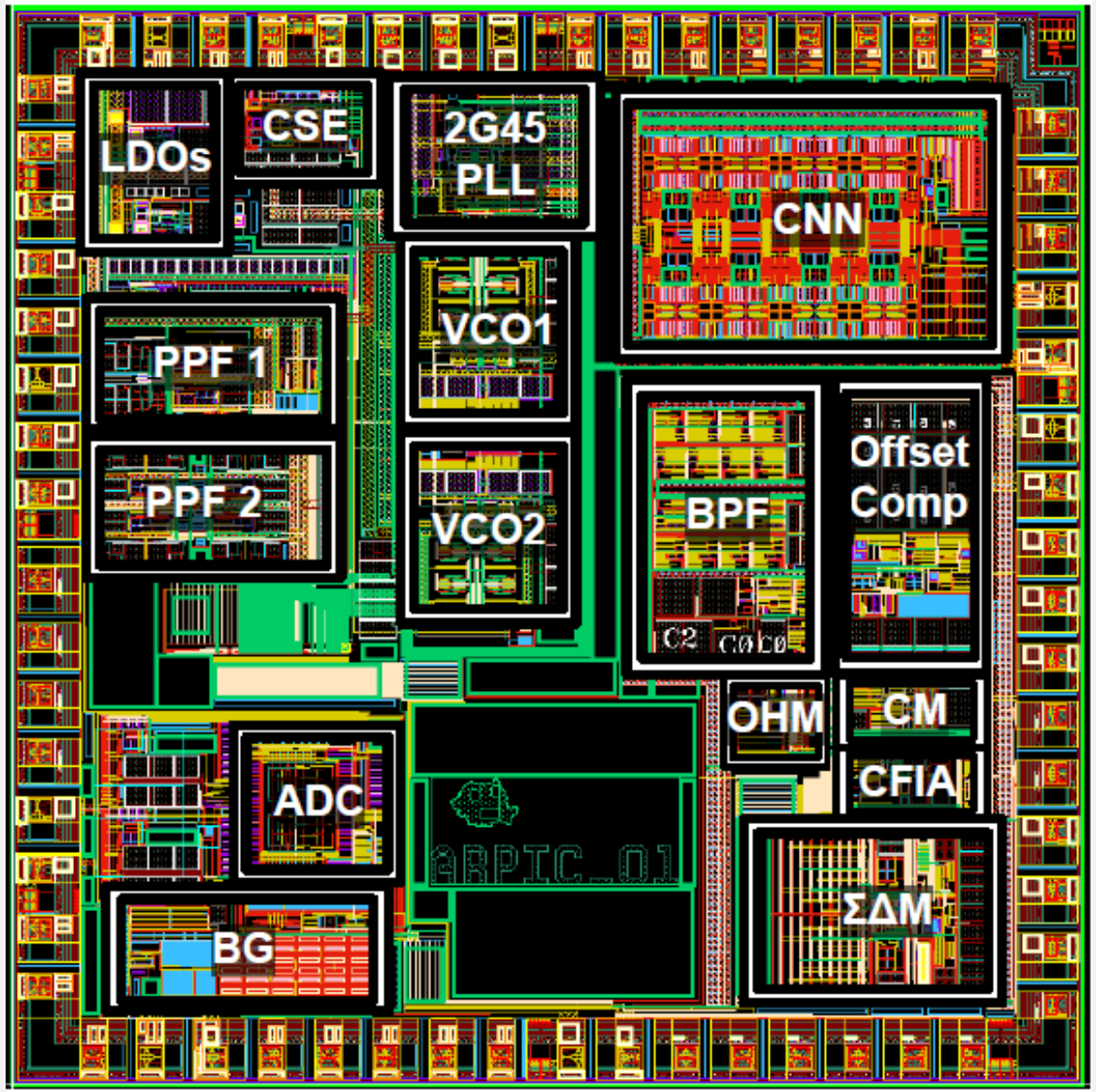
Faculty-to-IC designer career path based on scholarships:

- Scholarships provided by DERFAIC for undergraduate students
- MSc grants provided by our industrial partners

Or

- MSc and PhD students funded through active involvement in research projects

ARPIC_01



ARPIC = Romanian Academic Platform for IC Development: an open cooperation framework for joint development and silicon implementation of integrated circuits for teaching and academic research purposes

ARPIC01 = first modern analog IC designed exclusively by students and academics from three Romanian Technical Universities: Bucharest, Iasi and Cluj-Napoca

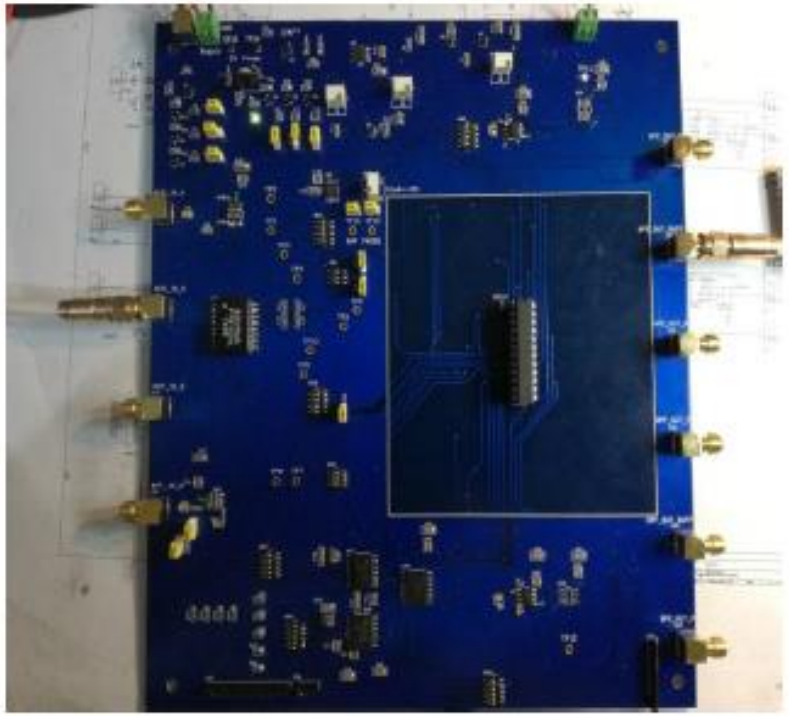
Blocks developed by the DERFAIC = Nord-West corner of the chip :

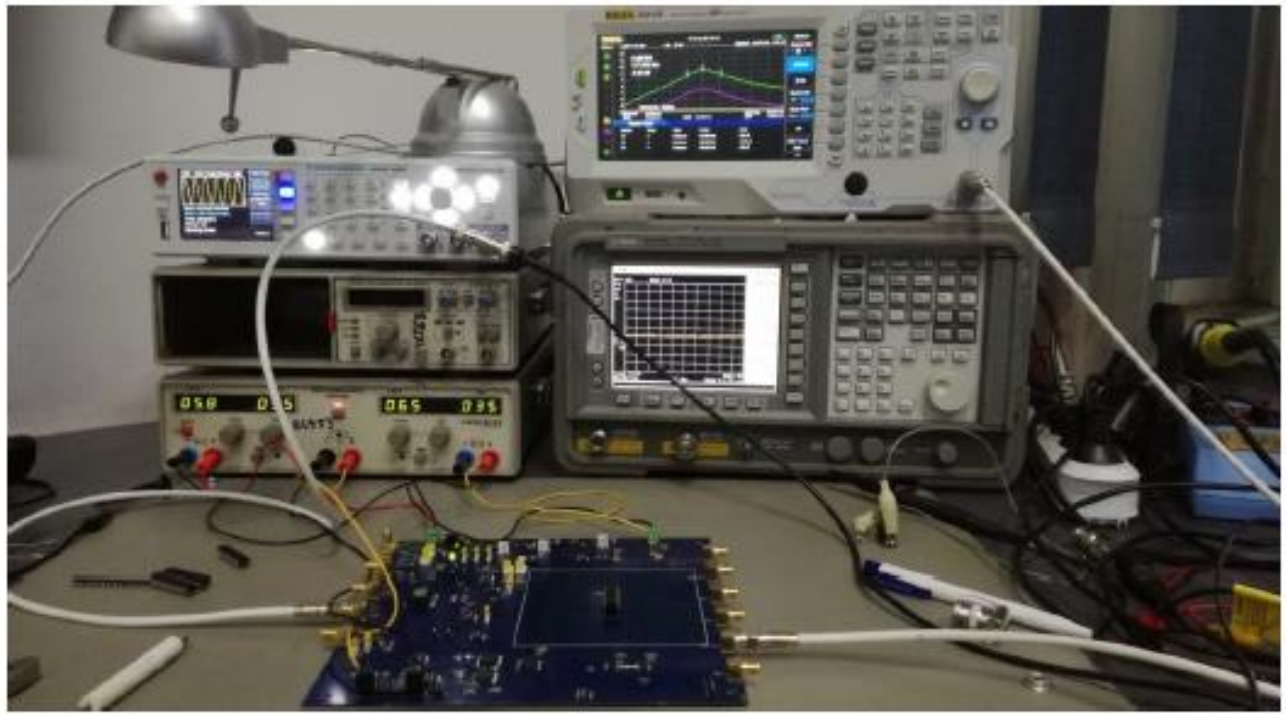
- Frequency synthesizer, Fmax = 2.45GHz
- Rail-to-rail voltage controlled oscillators (VCOs)
- Polyphase filters for image rejection in low-IF integrated radio receivers
- Low dropout voltage regulators (LDOs) with and without external decoupling capacitors
- High precision bidirectional current sensor

Integrated circuit for automotive applications: analog front-end for Hall sensor

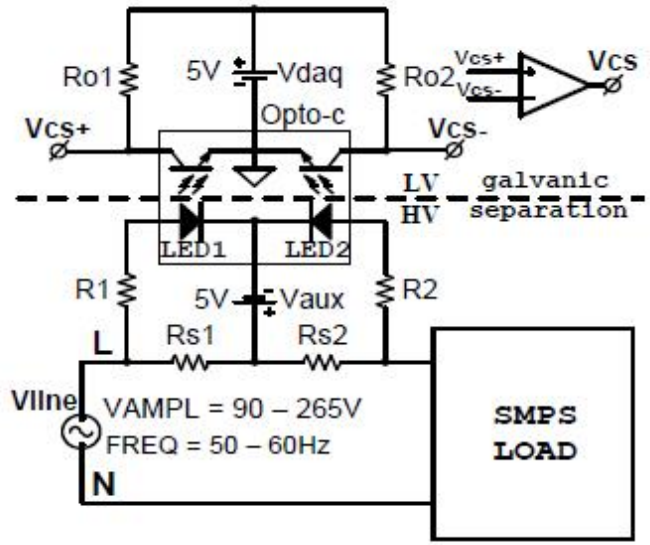
Aim: full design and characterization of an ASIC according to requirements set by the customer (a multinational IC design company, well known in automotive);
Main blocks: an instrument amplifier and a digitally-programmable bandpass filter. Two circuit implementations were completed for the instrument amplifier. Also included the usual auxiliary circuitry – bias, test, SPI.
Main results:

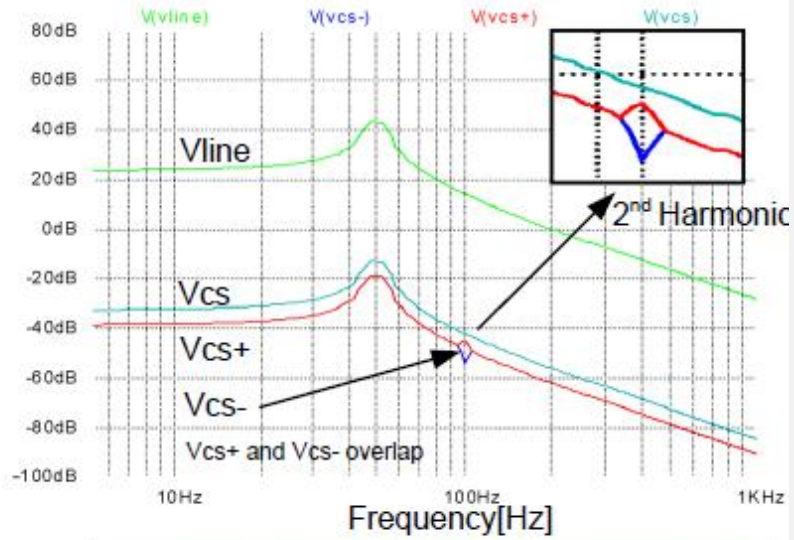
- 1st silicon fully functional and met the specs
- Test board designed and populated
- Complete IC characterization, including sensitivity wrt noise

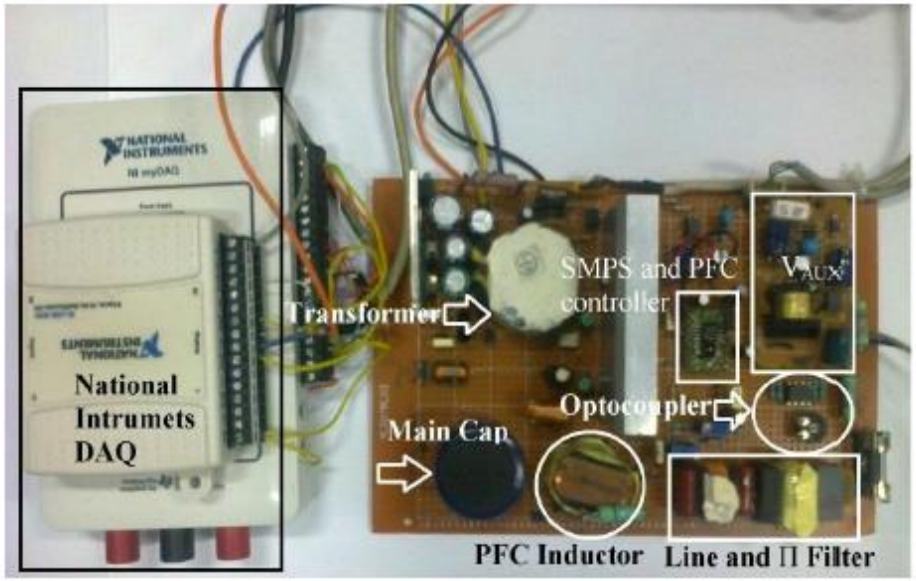


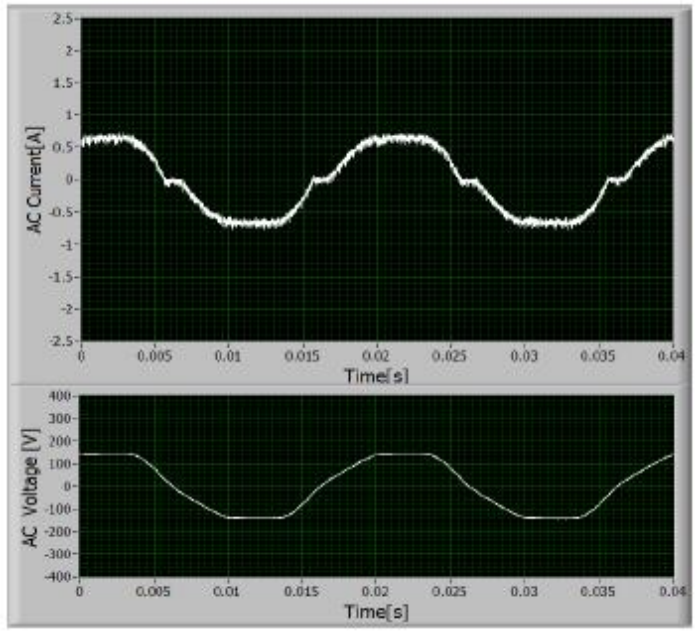


Current line sensor with matched optocouplers for active power factor correction

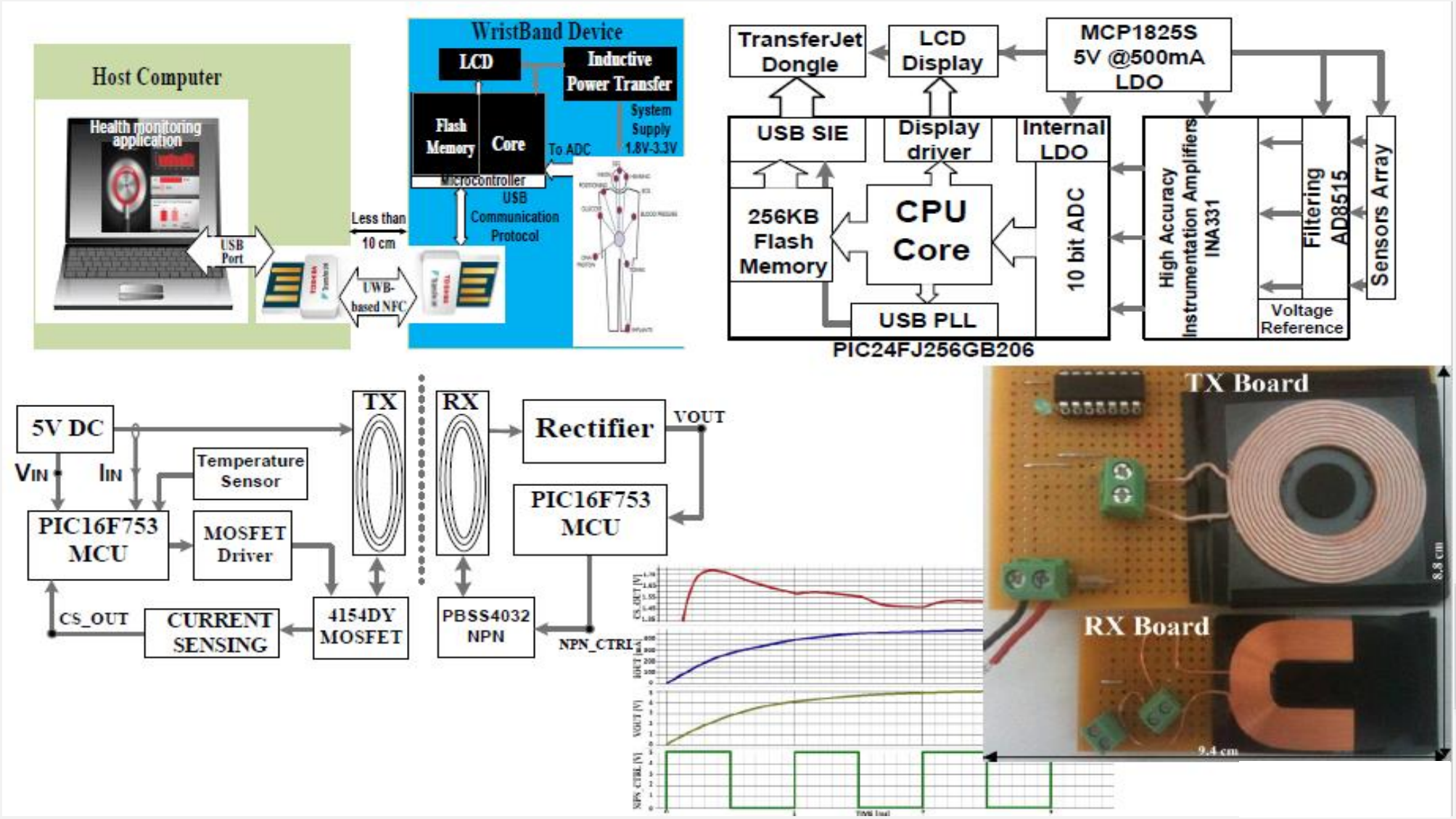






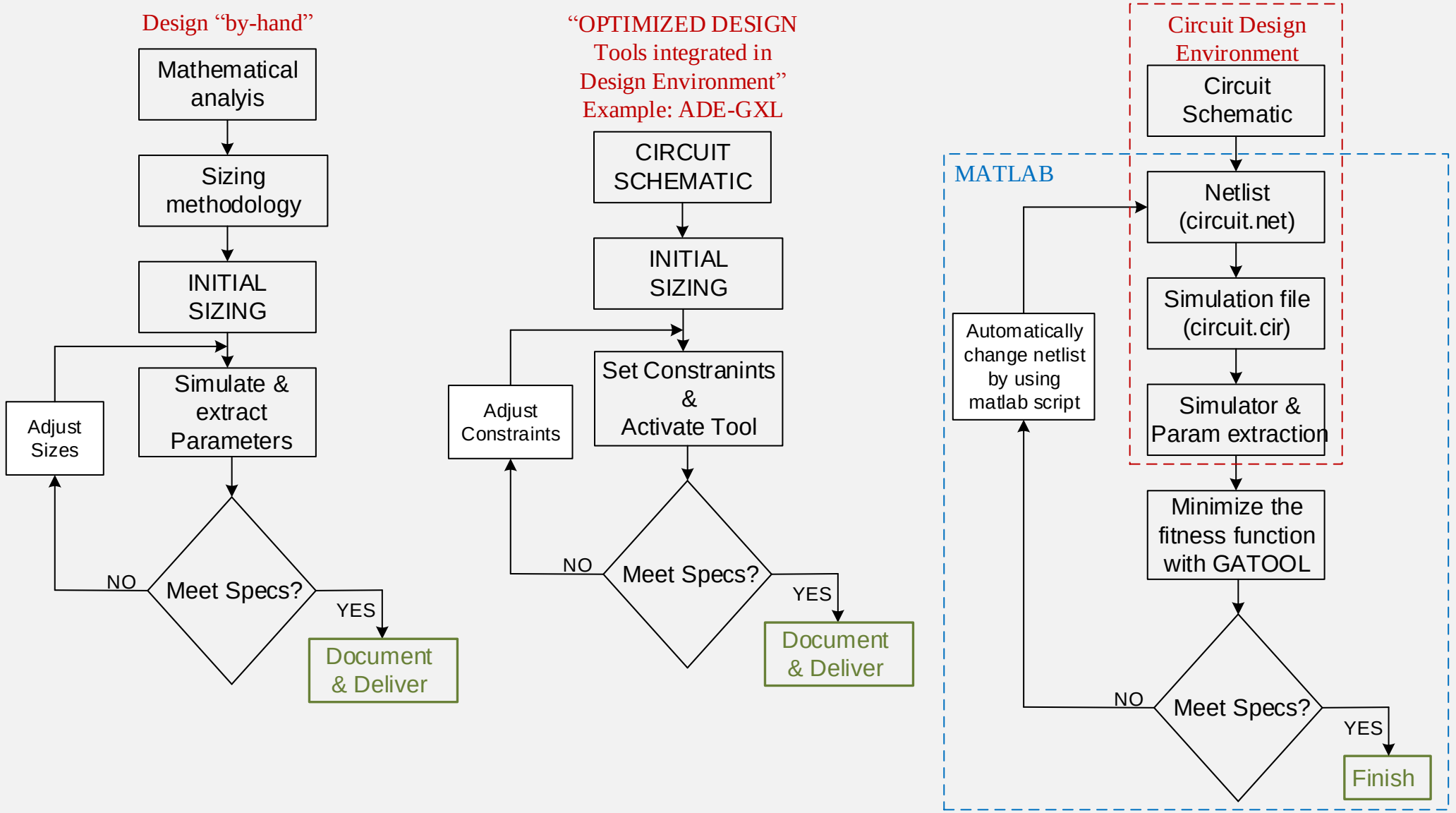


Wearable health monitor with NFC and inductive power transfer

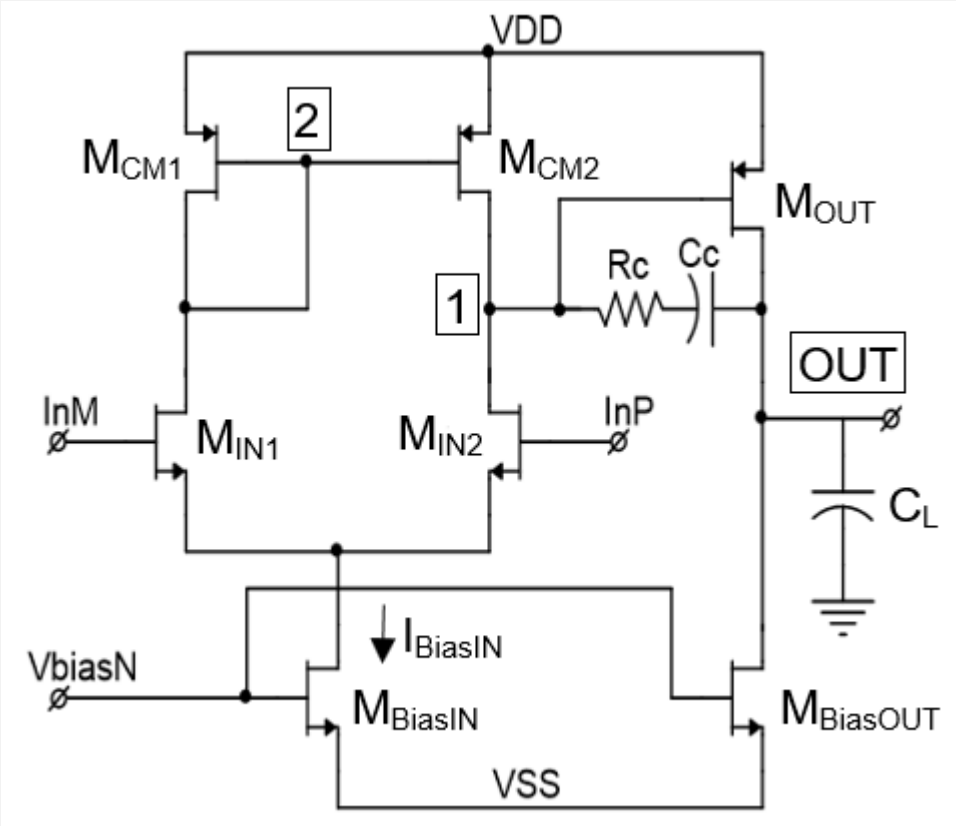


Approaches to optimized design illustrated by a simple example: the Miller OpAmp

Approaches to systematic and optimized design/sizing



Design Example: Standard Miller OpAmp with Rc-Cc compensation



Standard Miller OpAmp: Mathematical analysis

DC gain

$$A_0 = G_{mIN}G_{mOUT}R_{o1}R_{oOUT} = g_{mIN}g_{mOUT}(r_{DS\_IN}||r_{DS\_CM}) \cdot (r_{DS\_OUT}||r_{DS\_BiasOUT})$$

Dominant pole & GBW

$$f_{pole1} \approx \frac{1}{2\pi R_{o1}R_{oOUT}g_{mOUT}C_C}; GBW = A_0 \cdot f_{pole1} = \frac{g_{mIN}}{2\pi C_c}$$

Main secondary pole and zero

$$f_{Pole2} = \frac{g_{mOUT}}{2\pi C_L} \qquad f_Z^{Rc} = -\frac{1}{2\pi(1/g_{mOUT} - R_C)C_C}$$

Slew-Rate and max output voltage amplitude·frequency

$$SR = \min\left(\frac{I_{BiasIN}}{C_c}; \frac{I_{BiasOUT}}{C_L + C_c}\right); \; f_{OUT\_\max} \cdot V_{OUT_{\max}} < \frac{SR}{2\pi}$$

Offset voltage at the OA input, V_{OS}, & condition to minimize it

$$V_{OS} = f[V_{DSsatIN}, (W \cdot L)_{IN}, V_{DSsatCM}, (W \cdot L)_{CM}]; \; V_{DSsatCM} = V_{DSsatOUT}$$

Design Example: Standard Miller OpAmp with Rc-Cc compensation

Sizing Methodology

$C_C = 0.22 C_L$

$(1) \rightarrow g_{m1}$

$(2) \rightarrow I_{D1,2}$

$(3) \rightarrow SR$

$I_{D6} = I_{dd\_max} - 2 \cdot I_{D1,2}$

$Vdsat_6 \rightarrow Gm_2$

$(4,5) \rightarrow PM \rightarrow R_C$

$(6,7) \rightarrow A_0$

Start with same condition for Cc as the standard Cc-only approach but use Rc-Cc comp network

Eq. 1 => The transconductance of the input transistors gm1 obtained from GBW spec.

1st value for the input transistors bias current results from matching and linearity specs.

Verify that the resulting value for SR is equal (or larger) than the specified SR

The rest of the available (spec'ed) current is allocated to the second stage.

Based on Gm/Id curves determine the optimum Vdsat for maximum Gm2; check linearity

Calculate Rc considering the expressions (4) and (5) for fz and PM, respectively

Calculate remaining Gm values using (6); then find optimal L and W considering noise and matching requirements, as well as the DC gain

Specs

A_0

GBW

PM

SR

I_{dd_max}

C_L

Noise

v_{dsat_MIN}

$(W*L)_{MIN}$

Sizing Equations

$$GBW = \frac{G_{m1}}{2\pi C_C} \quad (1)$$

$$V_{OS} = F(v_{dsat1}, (WL)_1) \quad (2)$$

$$SR = \frac{2I_D}{C_C} \quad (3)$$

$$f_z = \frac{1}{2\pi(1/G_{m2} - R_C)C_C} \quad (4)$$

$$PM = 90 - arctg(GBW/f_{p2}) - arctg(GBW/f_z) \quad (5)$$

$$gm = \frac{2I_D}{Vdsat} \quad (6)$$

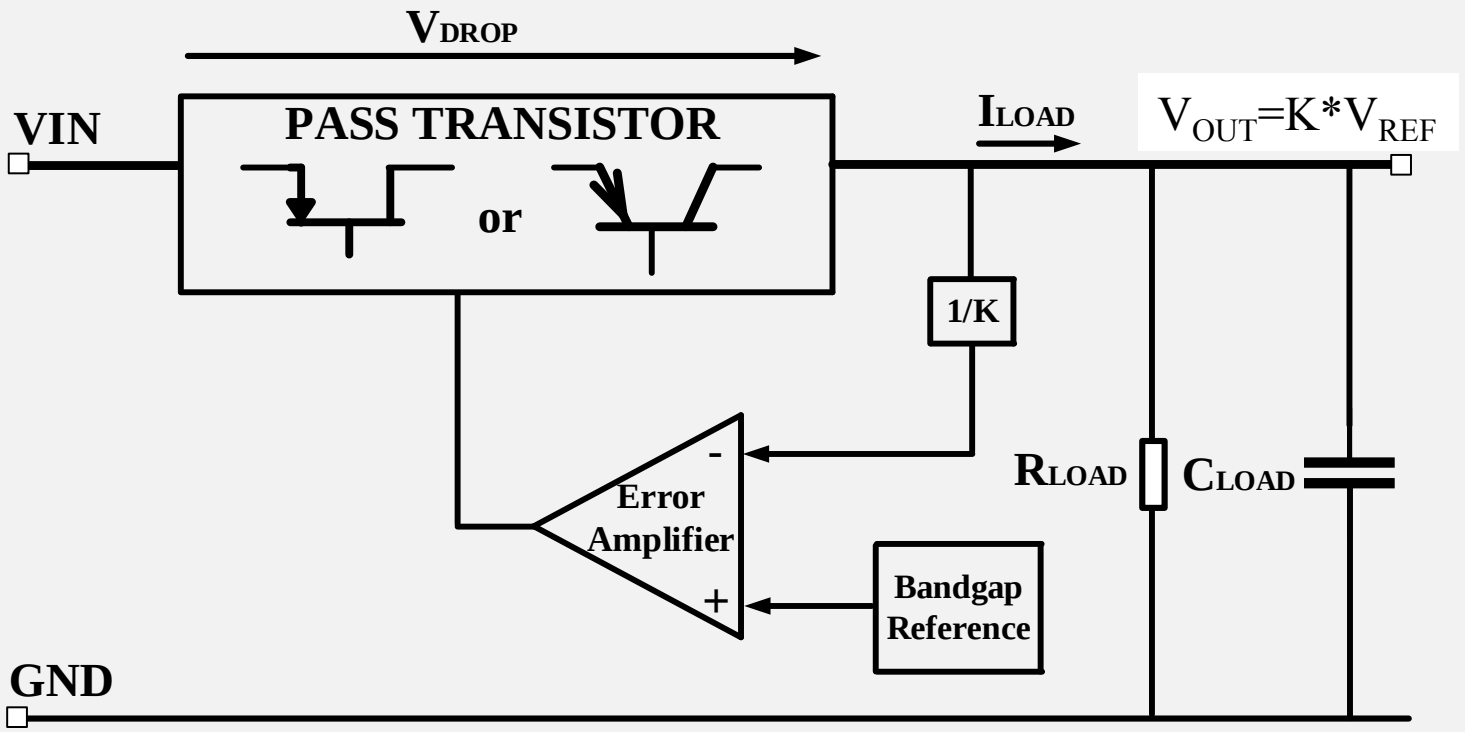
$$r_{DS} = \frac{V_E L}{I_D} \quad (7)$$

Design Example for Miller OpAmp: Student versus Optimization tools

Parameter	Specs	Student Design-by-hand 3 iterations	ADE-GXL, Initial = "Min"	ADE-GXL, Initial ="Student"	GA-based Optimization
Idd_max [uA] Vdd=1.2V	< 1000	750	870	940	850
DC gain [dB]	60	63.3	61	62.7	60.1
GBW [MHz] Cload=1pF	500	510	517	525	502
PhaseMargin [degrees]	>60	61	61.5	62.5	60.1
GainMargin [dB]	>10	21.6	17	23.2	16.5
SR [V/us]	150	155	162	175	150
Ripple of closed-loop response	<1dB	+0.7	-3	+0.25	-0.9

Examples of systematic design: LDOs developed by PhD students

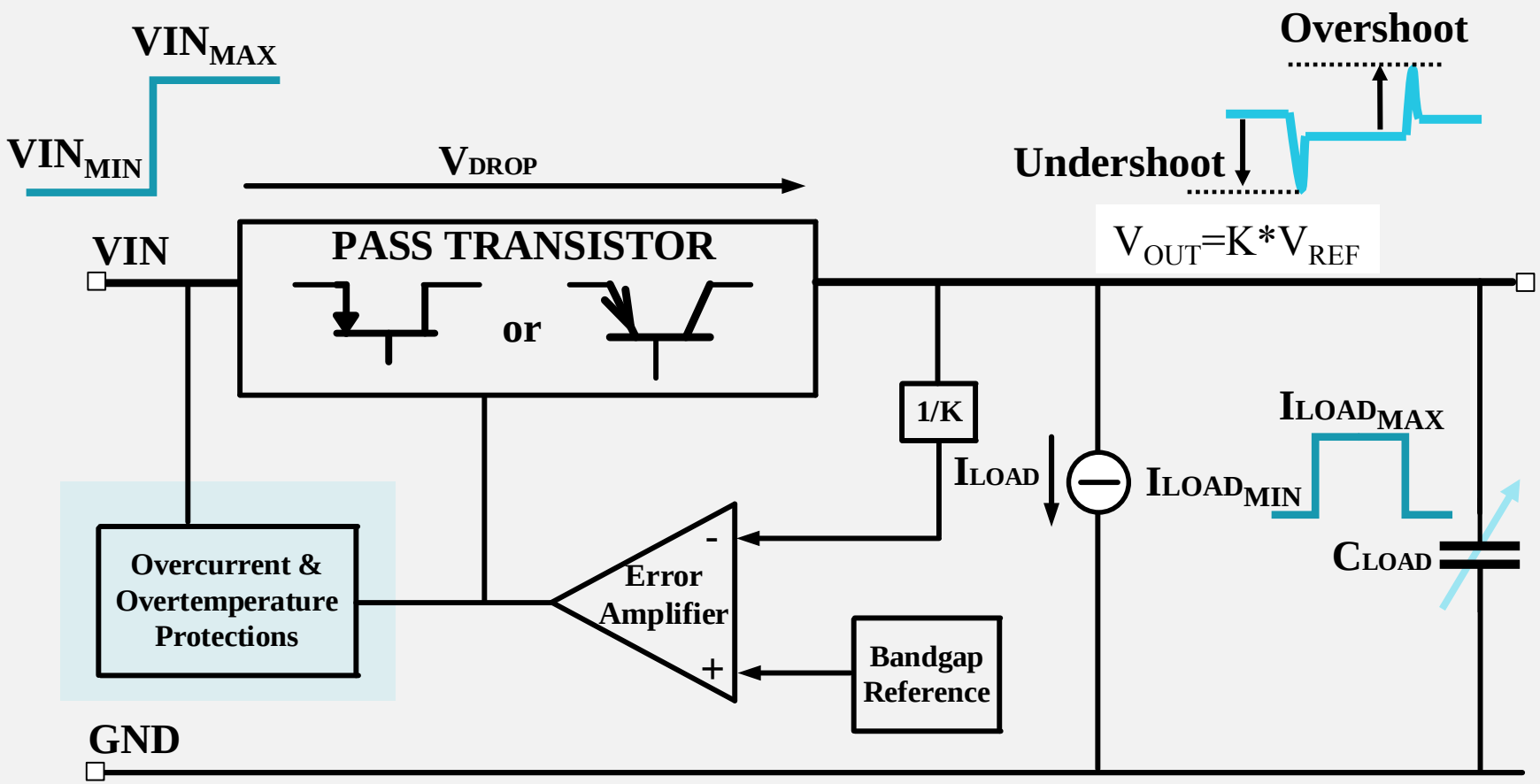
LDO: brief description and typical requirements



Typical requirements:

- Precise output voltage, insensitive to supply voltage and load current variations
- Low drop-out voltage
  VIN-VOUT = hundreds mV
- Small Quiescent Current
  IQ=uA – tens of uA

LDO: additional requirements and main design challenges



Typical requirements:

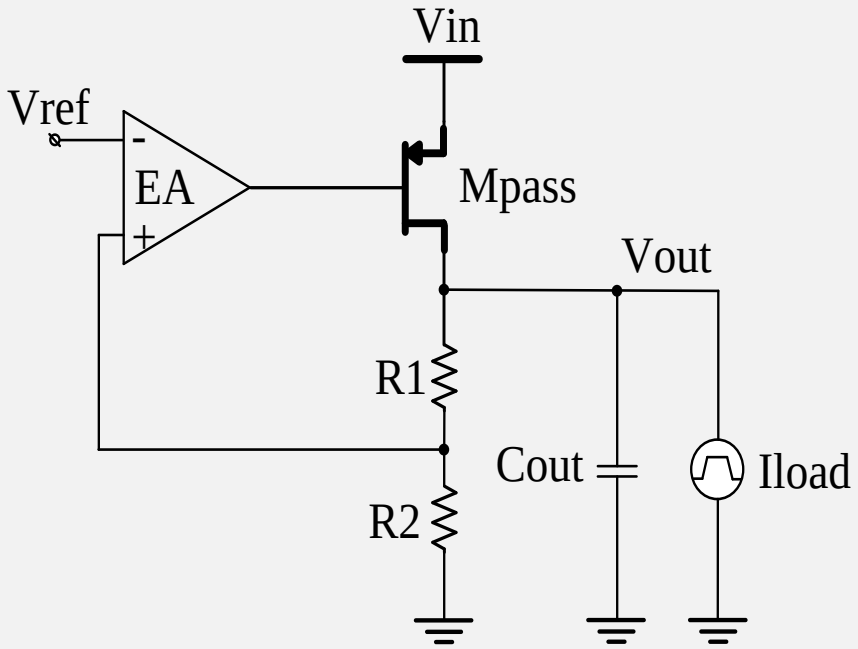
- Precise output voltage, insensitive to supply voltage and load current variations
- Low drop-out voltage
  VIN-VOUT = hundreds mV
- Small Quiescent Current
  IQ=uA – tens of uA

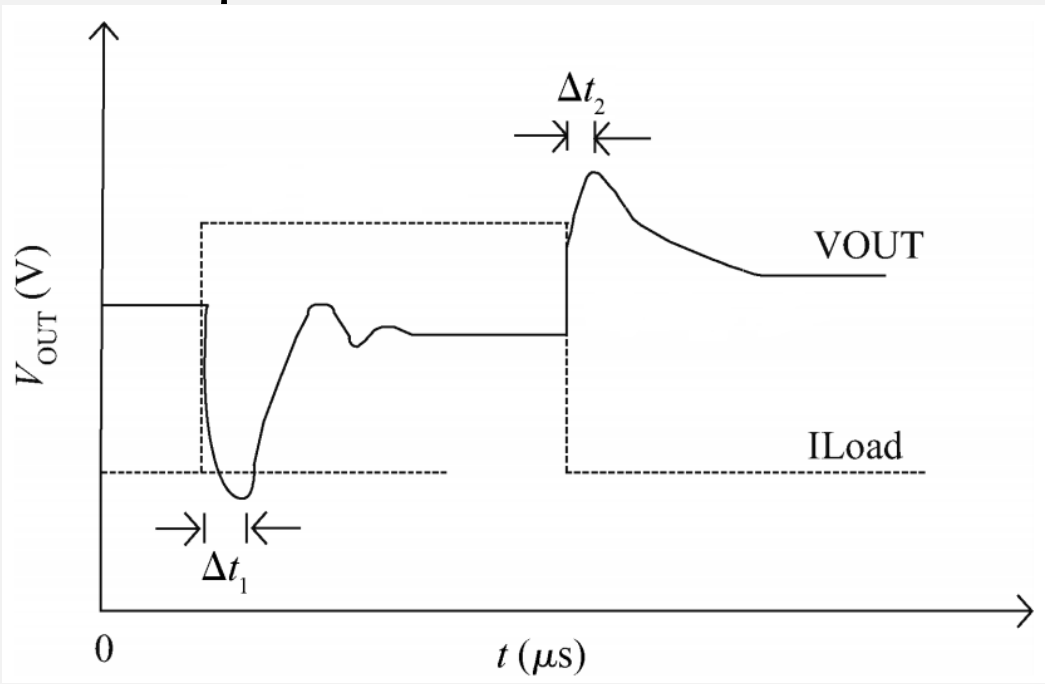
Additional requirements:

- Wide range of load currents
  ILOAD = 0 to hundreds mA
- Wide range of Cload (pF to uF)
- Fast response to steep variations of VIN and ILOAD
- Protection against abnormal operating conditions

Error Amplifier: Increasing SR for faster response to steep variations of I_{Load}

- Parameters that influence the load transient response of an LDO





$$V_{undershoot} \cong \Delta t_1 \frac{I_{max}}{C_{out}}; \quad \Delta t_1 \cong t_{SR1} + \frac{1}{BW_{cl}} = \frac{\Delta V C_{par}}{I_{SR1}} + \frac{1}{BW_{cl}}$$

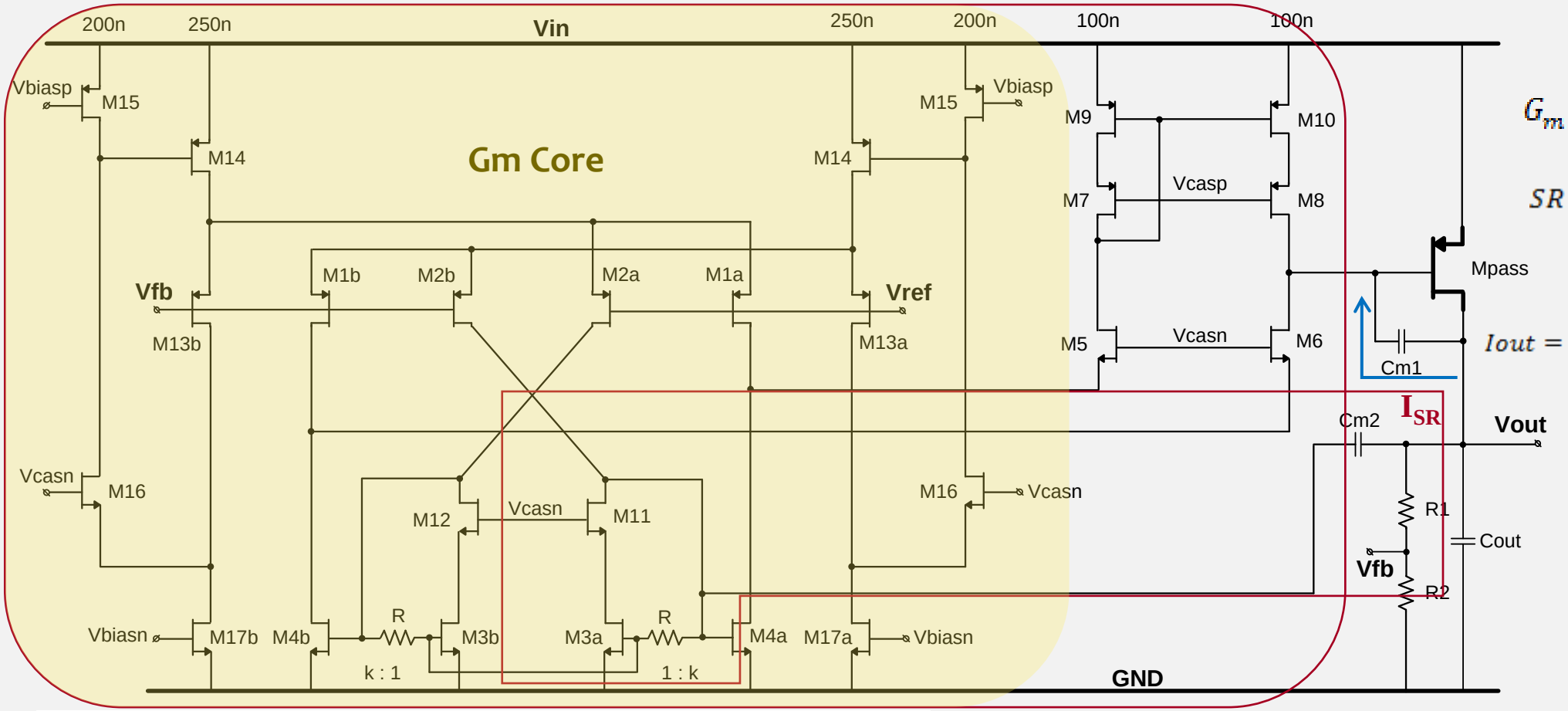
$$V_{overshoot} \cong \Delta t_2 \frac{I_{max}}{C_{out}}; \quad \Delta t_2 \cong t_{SR2} + \frac{1}{BW_{cl}} = \frac{\Delta V C_{par}}{I_{SR2}} + \frac{1}{BW_{cl}}$$

SR enhancement techniques

difficult to increase

Error Amplifier: Increasing SR for faster response to steep I_{Load} variations

- Super Class-AB Recycling Folded Cascode



$$G_m = g_{m1a}(1+k)$$

$$SR = \frac{2kI_B}{C_L}$$

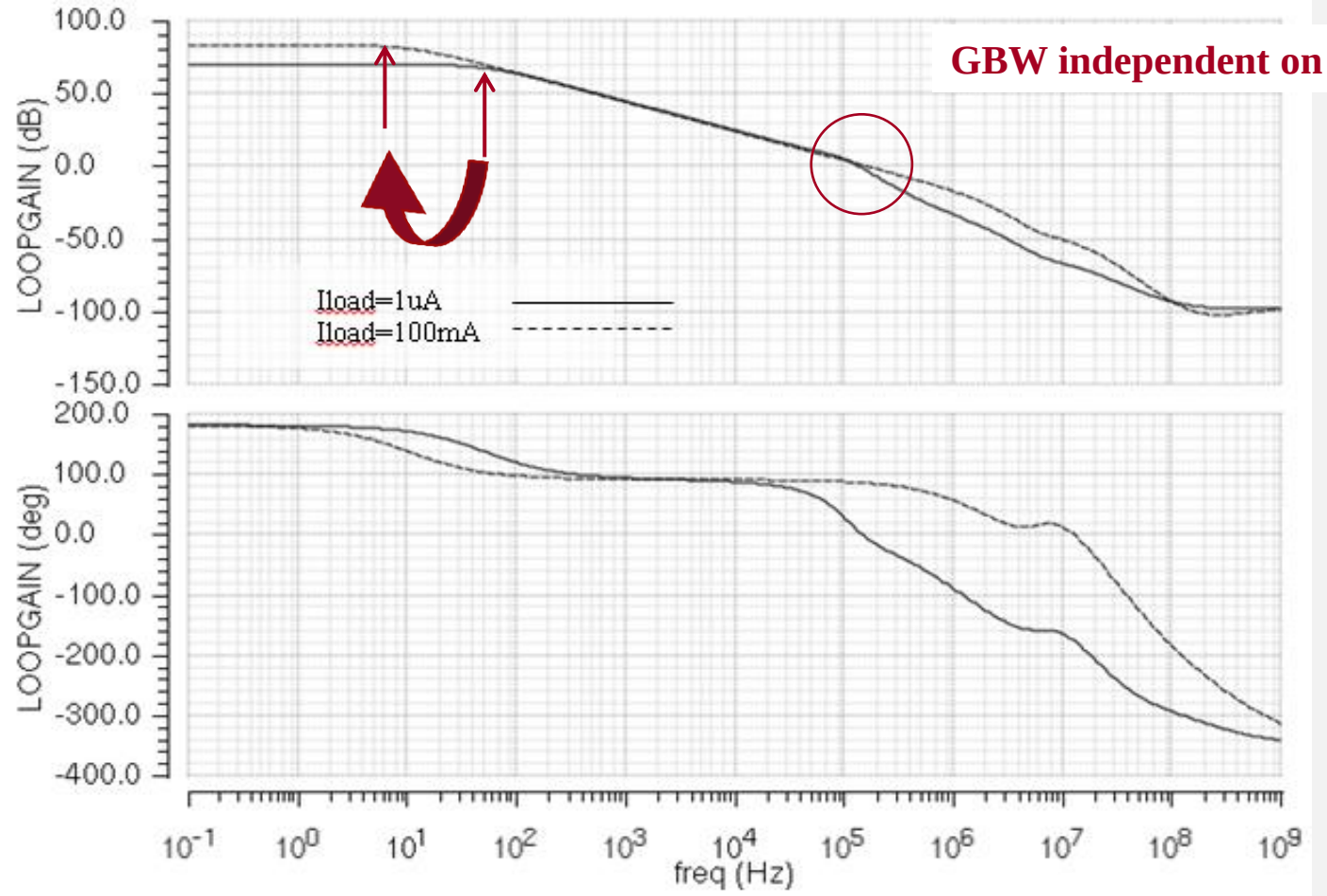
$$Iout = \pm \frac{\beta_{4a,4b}}{2}\left(\sqrt{\frac{2I_{cm}}{\beta_{3a,3b}}} + \frac{R|I_d|}{2}\right)^2$$

SR enhancement techniques:
- **Current recycling**
- **Adaptive Biasing using cascoded Flipped Voltage Follower**

Capacitor multiplier technique to create dominant pole

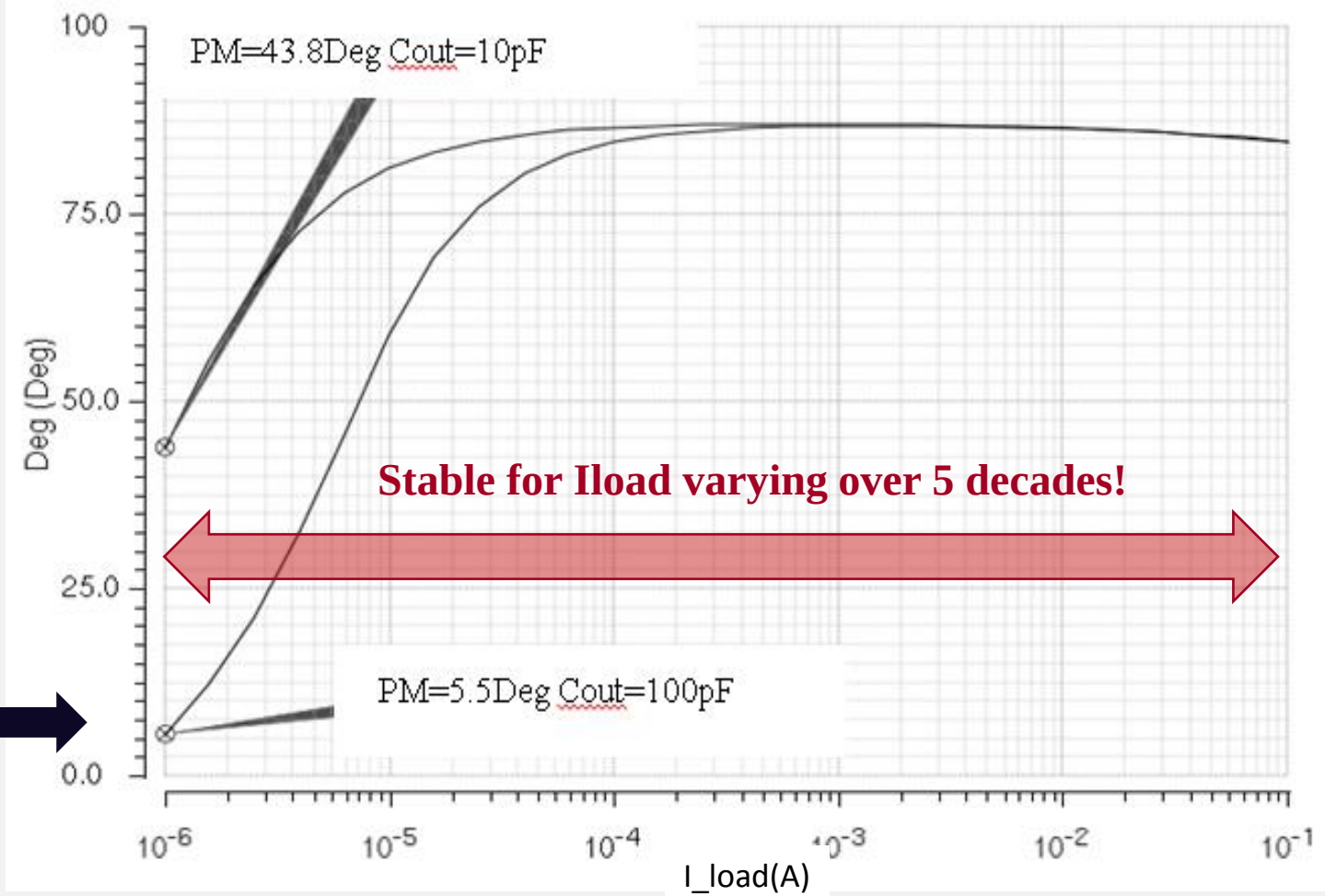
LDO: Simulation Results

- Small-signal analysis: Loop gain variation with I_{load}



LDO: Simulation Results

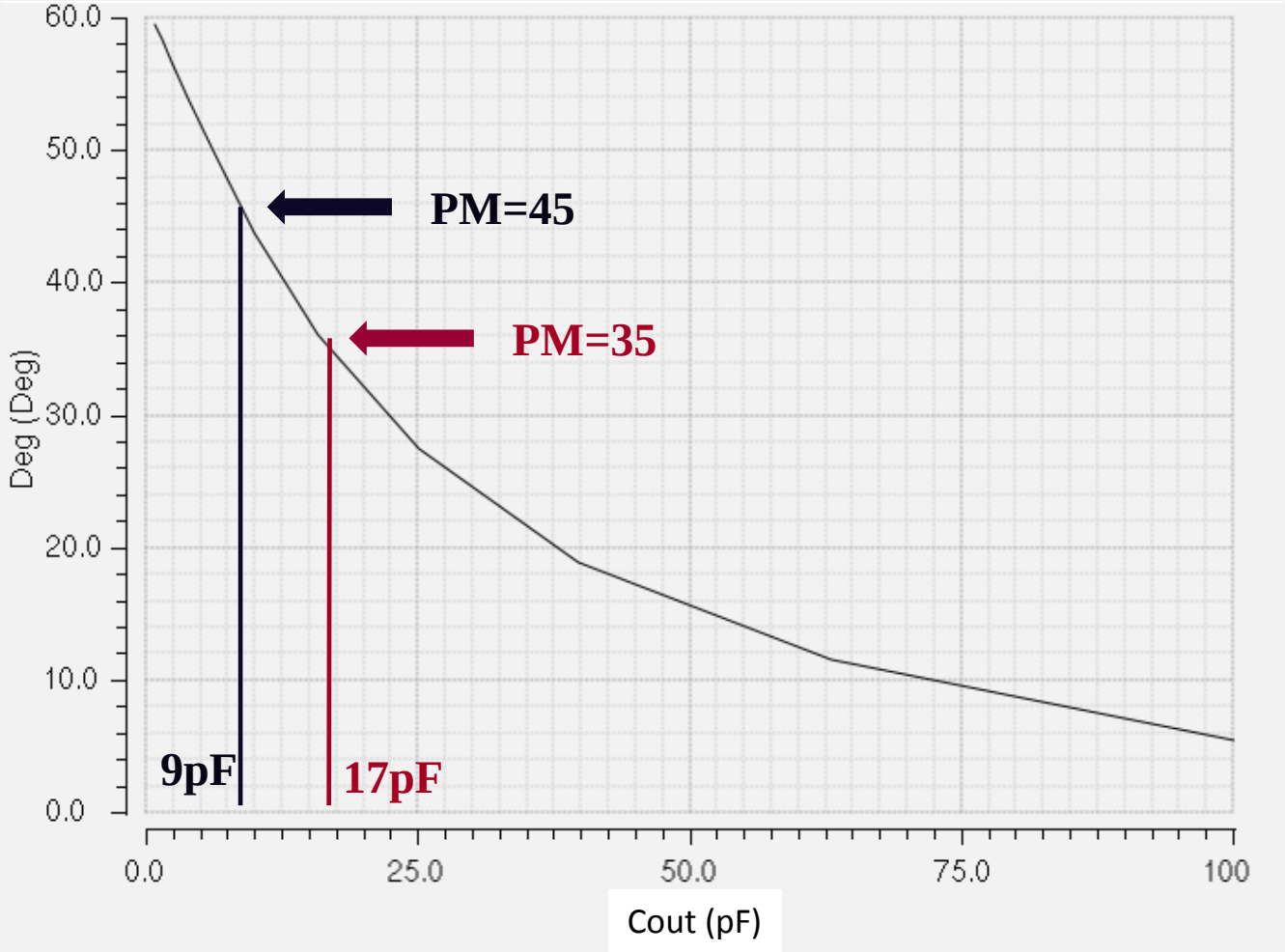
- Small-signal analysis: PM variation with I_{load}



Small PM but acceptable for this application

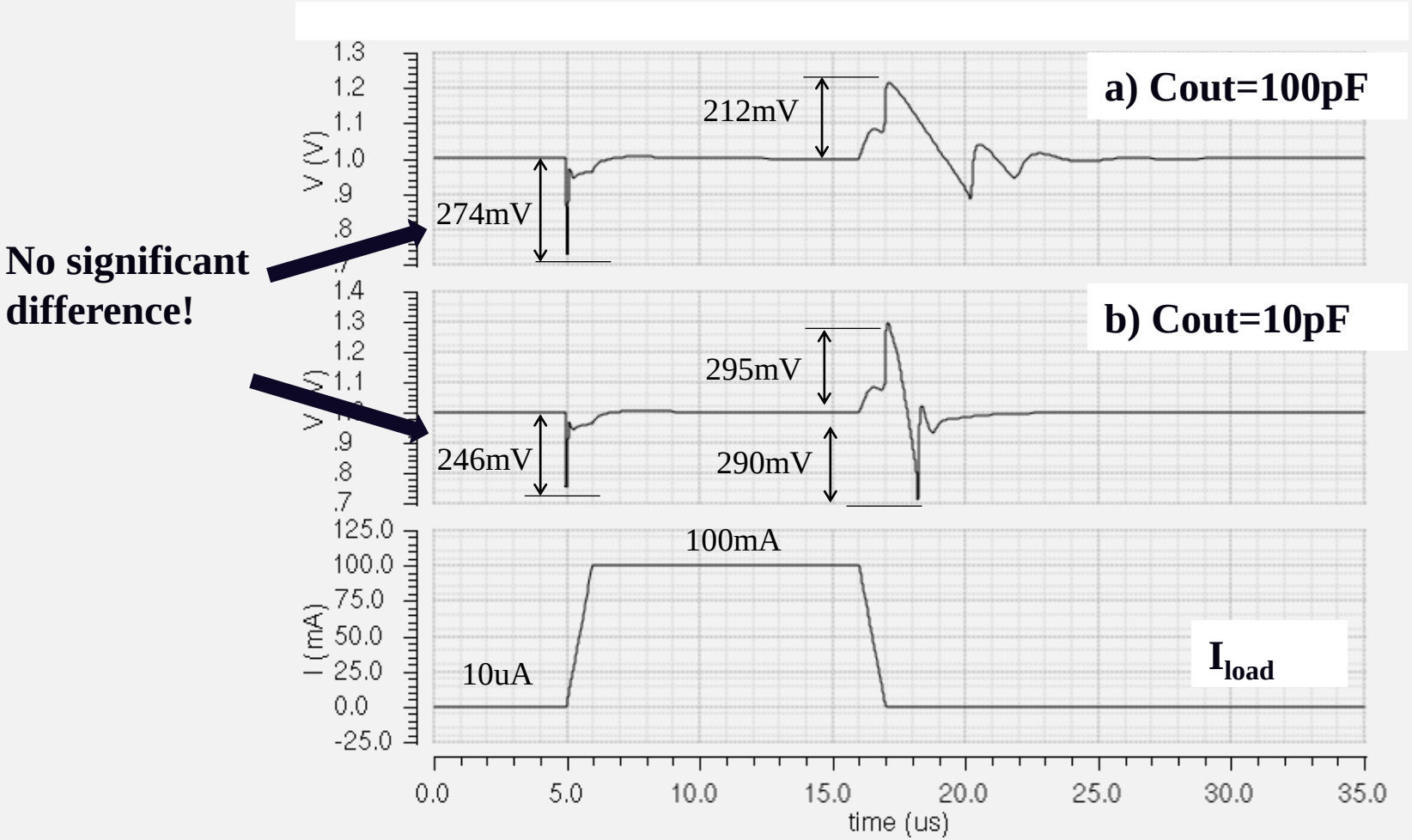
LDO: Simulation Results

- Small-signal analysis: PM variation with Cout @ small I_{load}



LDO: Simulation Results

- Load transient response (I_{load} step from 10uA to 100mA, $t_{rise}=t_{fall}=1us$):

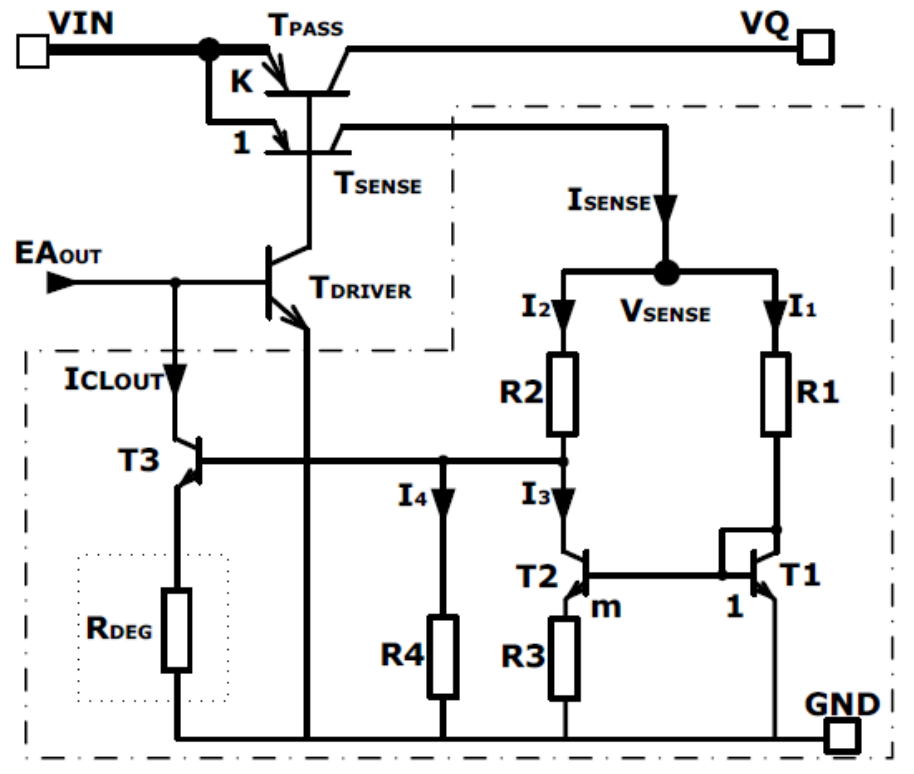


LDO: comparison between different topologies

Parameter	Wang -2010	Saberkari – 2013	Ming - 2012	Recycled folded-cascode CAS2015
CMOS (µm)	0.35	0.18	0.35	**0.18**
Supply Voltage (V)	4-6	1.2	2.5-4	**1.8**
Output Voltage (V)	2.5	1	2.35	**1**
Dropout Voltage (mV)	200	200	150	**90**
Iout (mA)	250	100	100	**100**
Iq (µA)	20	3.7	7	**1.12**
Cout (pF)	100000	100	10-100	**0-100**
Response Time (ns)	N.A	N.A.	N.A	**30**
ΔVout (mV)	110	277	236	**274**
Line regulation (mV/V)	2	N.A.	1	**0.077**
Load regulation (mV/mA)	0.04	N.A.	0.08	**0.0028**
FOM (fs) (Cout=100pF) FOM = $\frac{\Delta V_{Out} C_{out} I_q}{I_{out\ max}^2}$	3520	10.2	16.5	**3.1**

Over-current protection

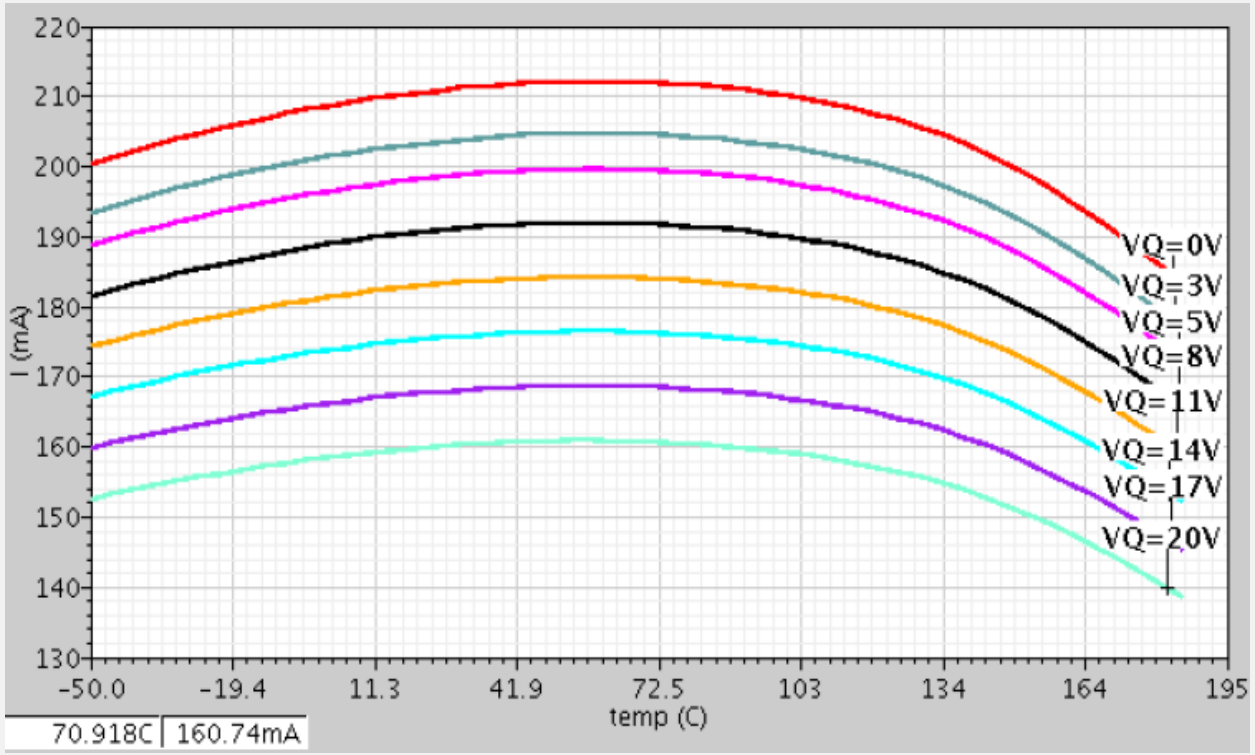
- Proposed implementations



$$I_{SENSE_{TRIP}} = \left[\left(\frac{V_T \ln m}{R_3} + \frac{V_{BE3}}{R_4}\right) \cdot \left(1 + \frac{R_2}{R_1}\right)\right]$$

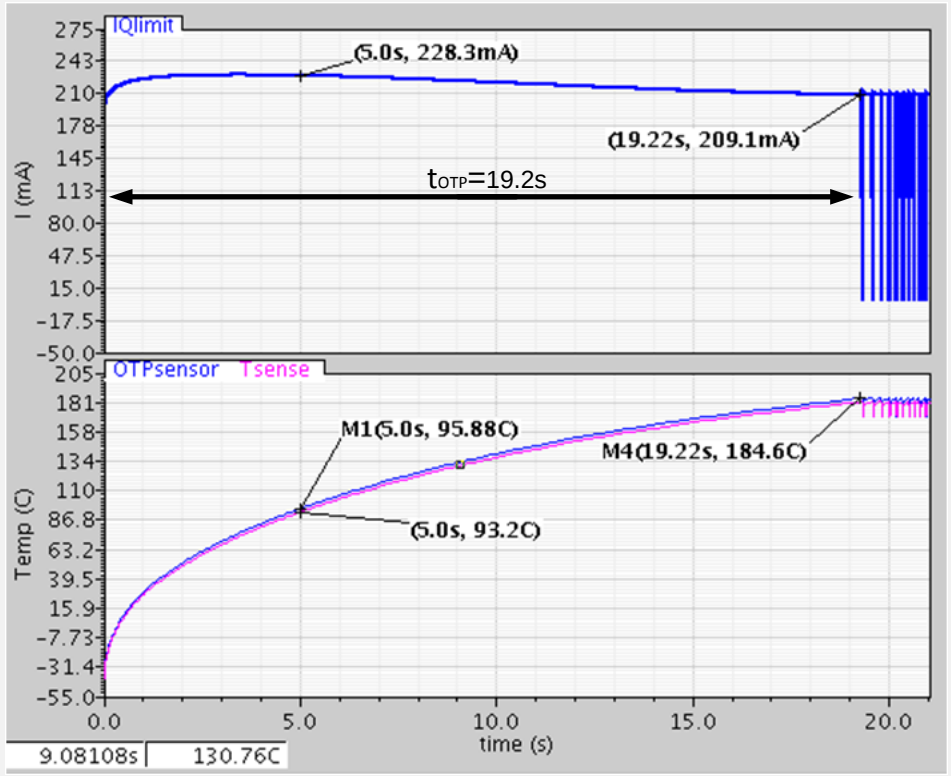
$$I\_Limit = K \cdot I_{SENSE_{TRIP}} \cdot \frac{\left(1+\frac{VIN-VQ}{V_A}\right)}{\left(1+\frac{VIN-V_{SENSE}}{V_A}\right)}$$

- Simulations Results

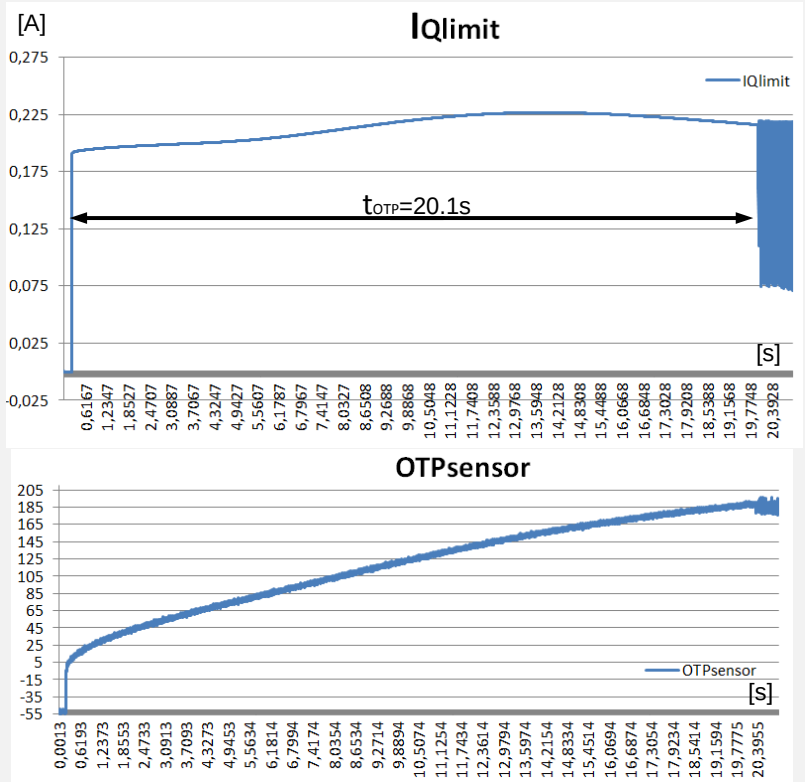


Over-current protection: Electro-thermal simulations versus measurements

➢Electro-thermal simulations results



➢Measurements results

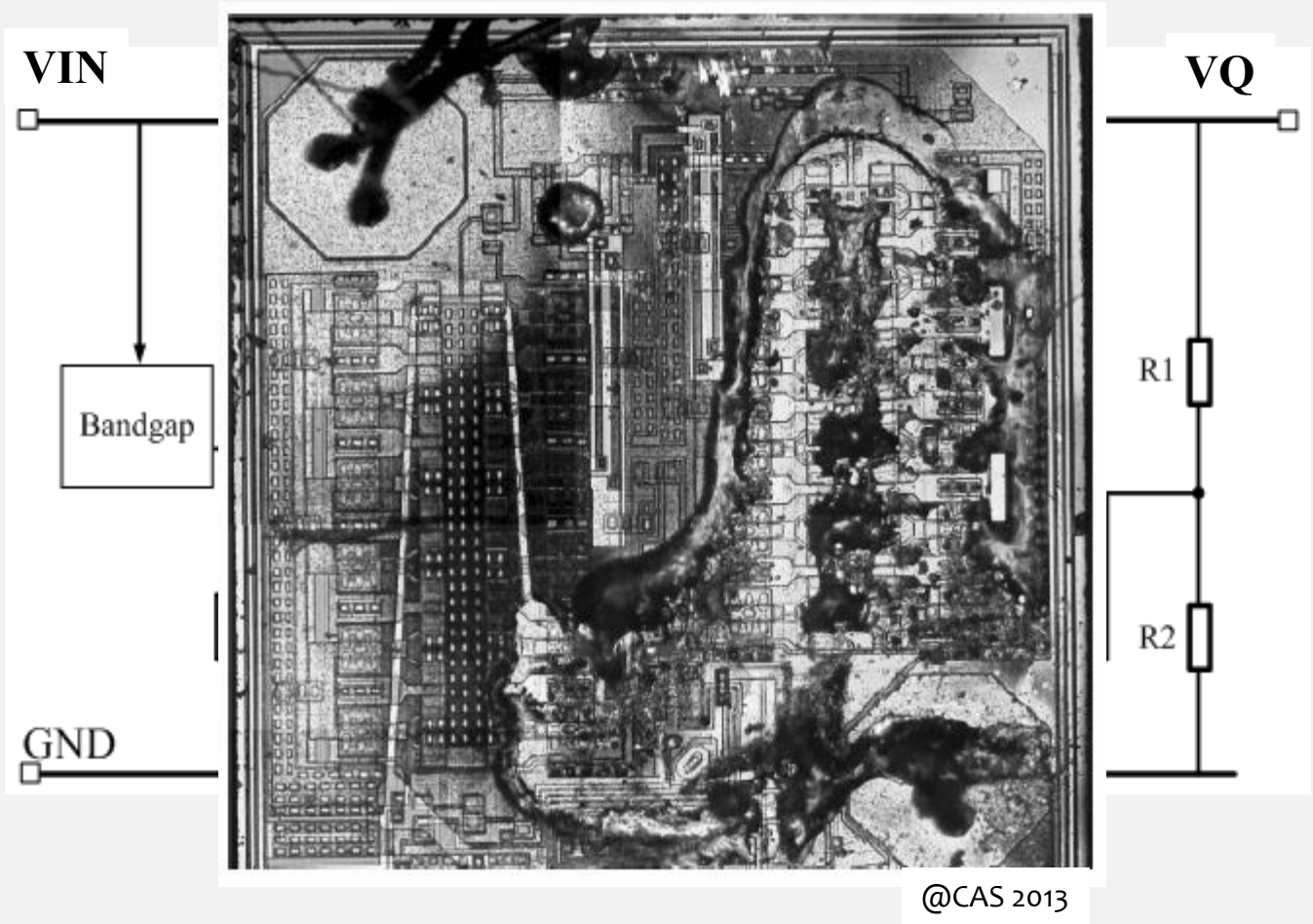


➢The maximum value of I_Limit is almost the same for measurements and for the electro-thermal simulations, 223mA as against 228mA (both sims and measurements performed in the same scenario).

➢The dynamic behavior of the LDO is also in good agreement. The time until the over-temperature protection is activated (t_{OTP}) has a small variation, of 5% between the measurements – 20.1s and electro-thermal simulations – 19.2s

Over-temperature protection: brief description and main requirements

➢ Block Diagram



@CAS 2013

Main Requirements

1. The maximum temperature allowed within the LDO

➔ Set activation temperature threshold considering the thermal coupling.

➔ Optimal placement of the temperature sensor

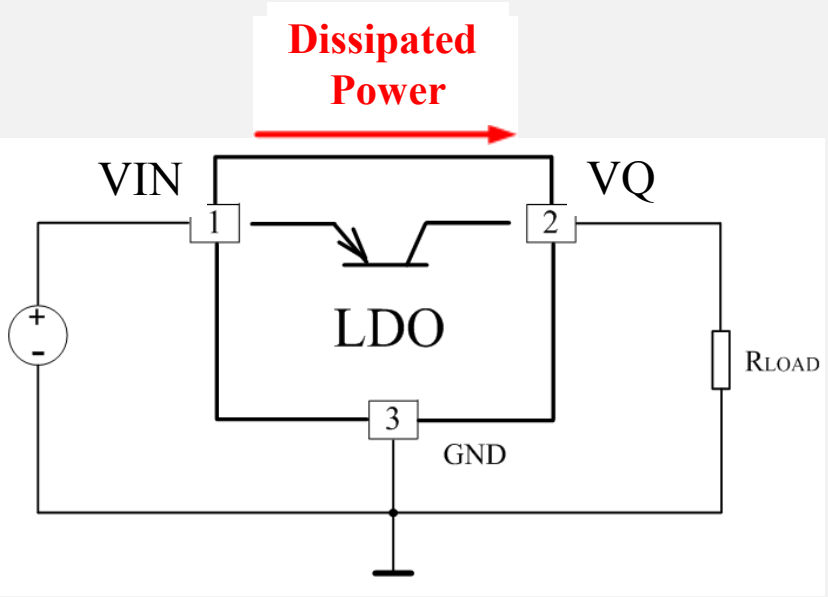
2. Hysteretic characteristic to prevent false triggering

➔ Set the deactivation temperature threshold considering wanted hysteresis width

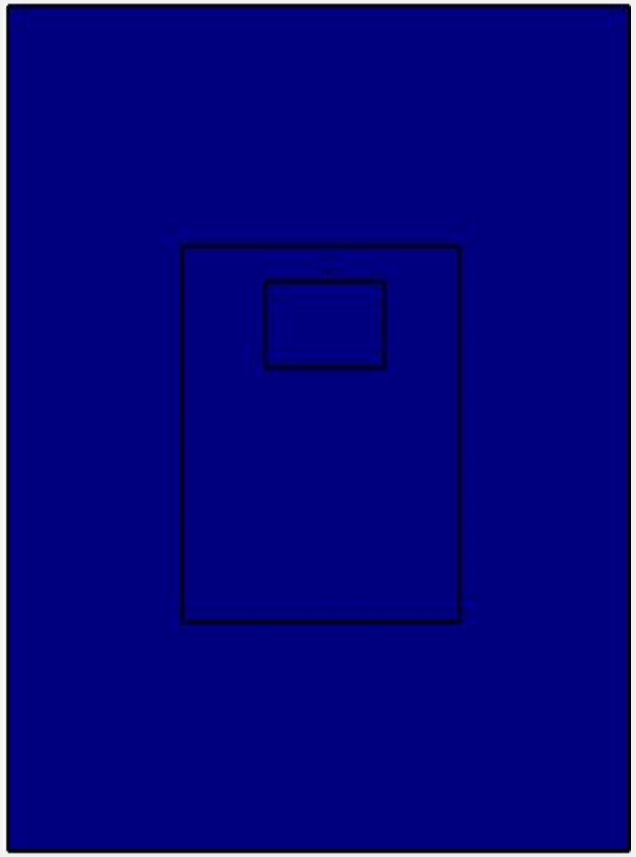
3. Check operation under worst case dynamic test scenario (Start-up with shorted-output).

Over-temperature protection: design based on electrical and thermal-only sims

➢ Main ideas



- Thermal Impedance
- Thermal Coupling
- Thermal Map



➢ Shortcomings

- The thermal-only simulations assume that the electrical parameters of the circuit do not change when the temperature varies due to the applied power

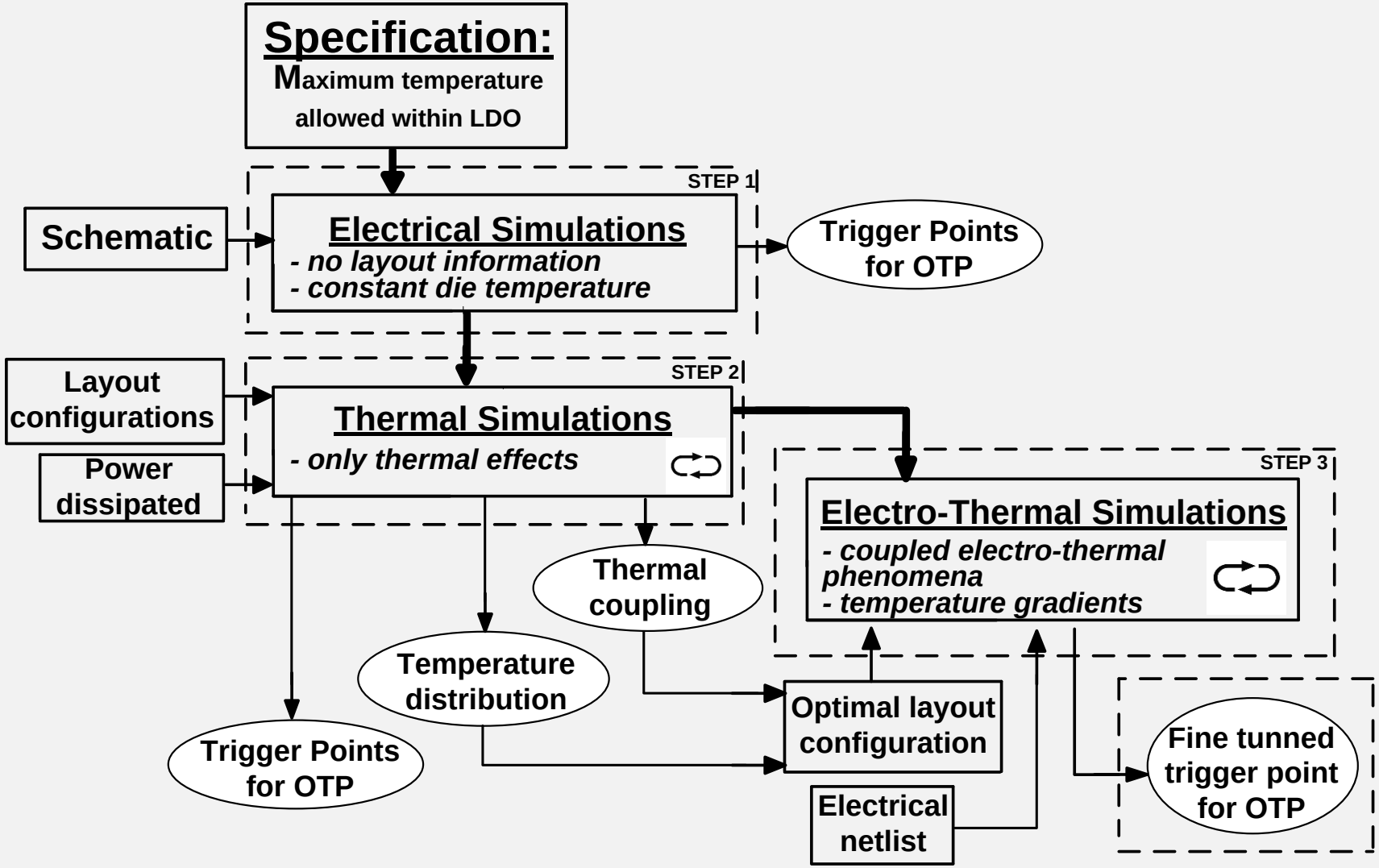
- Standard electrical-only simulations assume that all the devices within a chip operate at the same temperature

- The variation in time of the temperature distribution cannot be revealed by performing thermal only simulations – this could cause damage of the circuit

- The dependency between the initial conditions (different scenarios regarding the polarization of the circuit) and the temperature distribution can be fully covered only by performing electro-thermal sims

Over-temperature protection: design methodology based on electro-thermal sims

➢ Flow-chart of the methodology proposed to design OTP circuitry



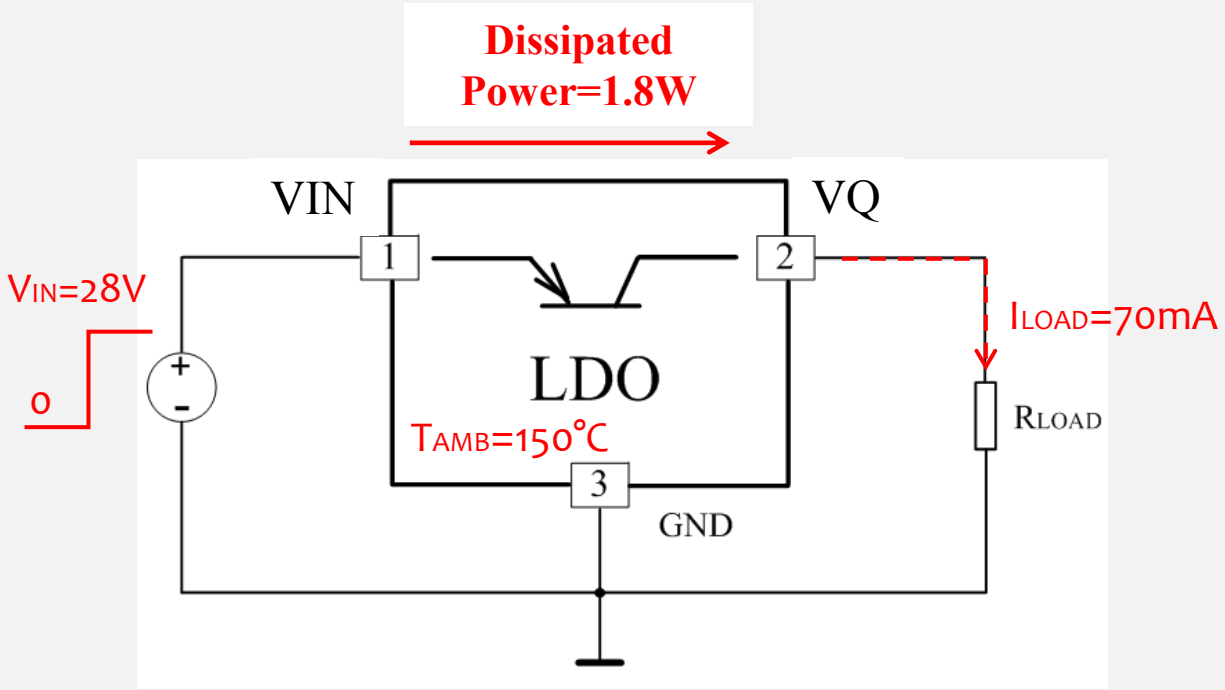
Over-temperature protection: design methodology based on electro-thermal sims

- Design Example

Requirements

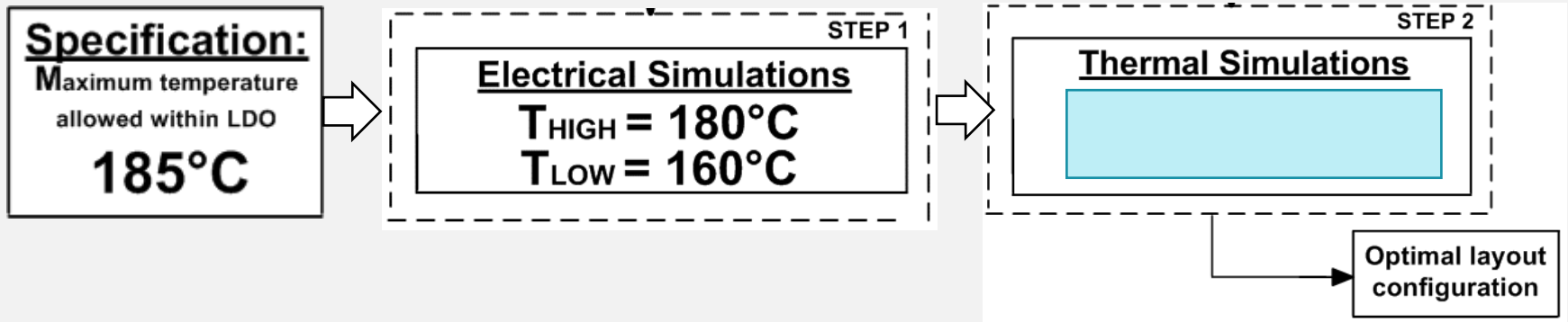
Specifications:	
Maximum temperature allowed within LDO	Hysteresis Width
185°C	>15°C

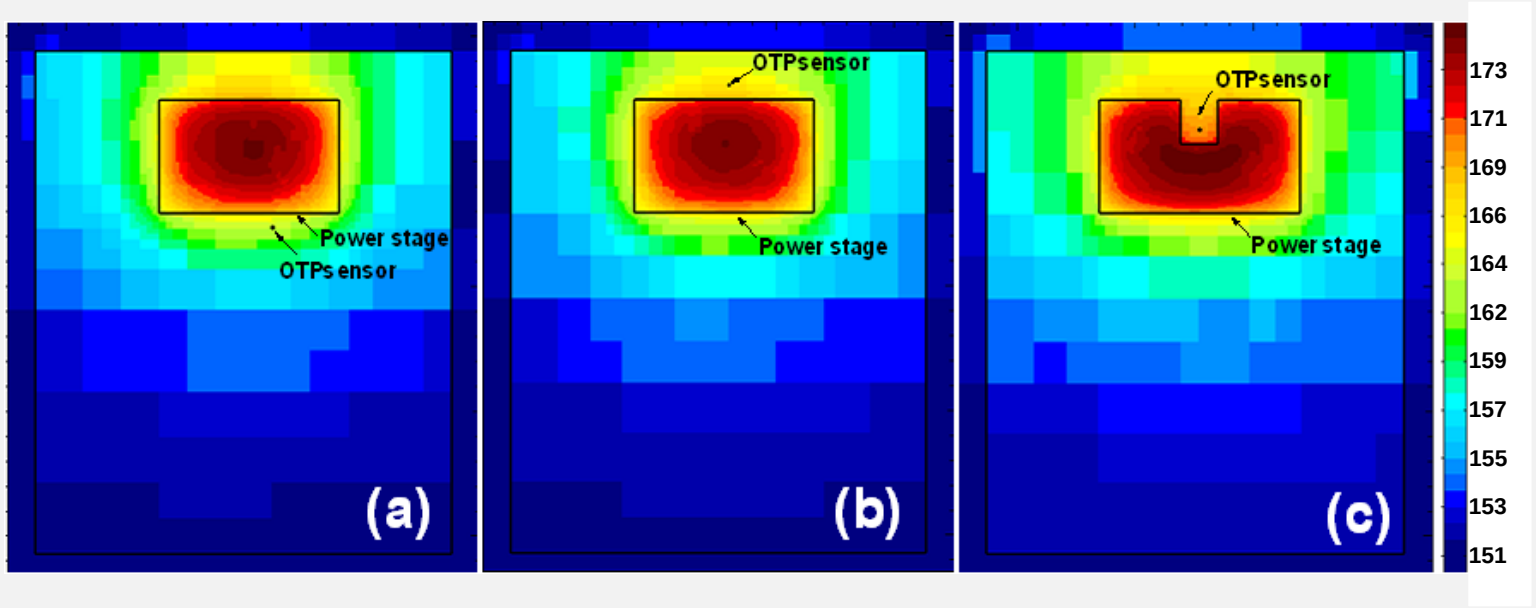
Scenario



Over-temperature protection: design methodology based on electro-thermal sims

- Steps 1 & 2: Electrical-only and Thermal-only sims



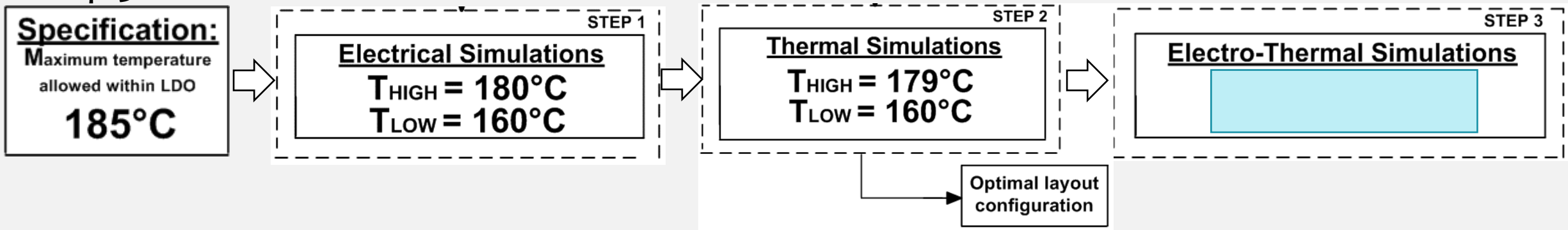


	DeltaT [°C]	
	T_{AMB}=-40°C	T_{AMB}=150°C
TSD sensor below	14	12
TSD sensor above	9	8,7
TSD sensor in a notch	6	5,8

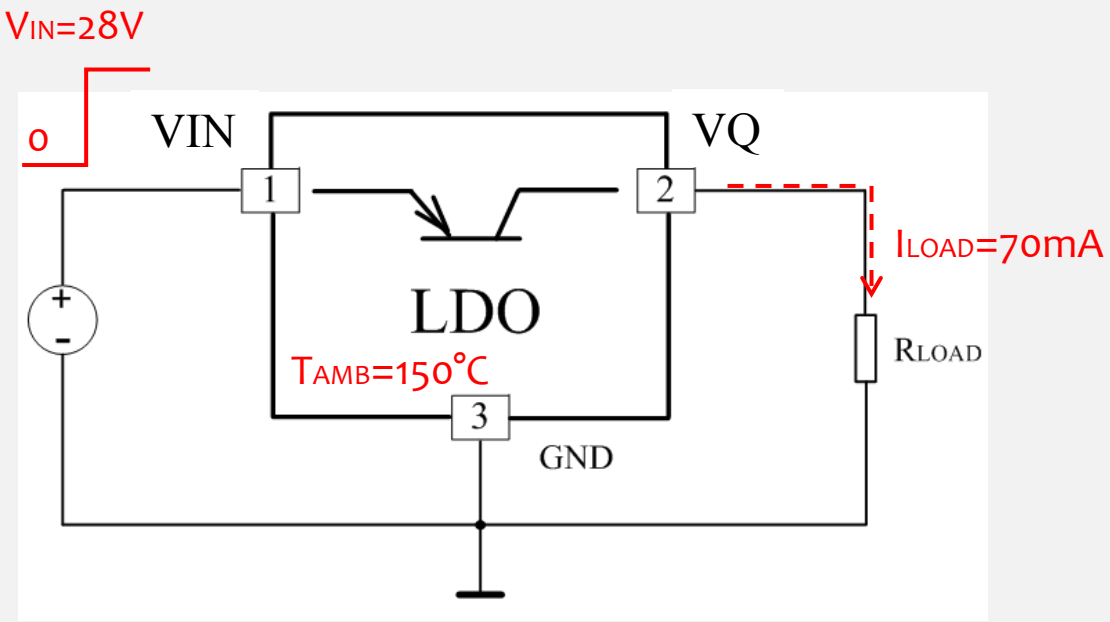
*$P_{APPLIED}$=1.8W

Over-temperature protection: design methodology based on electro-thermal sims

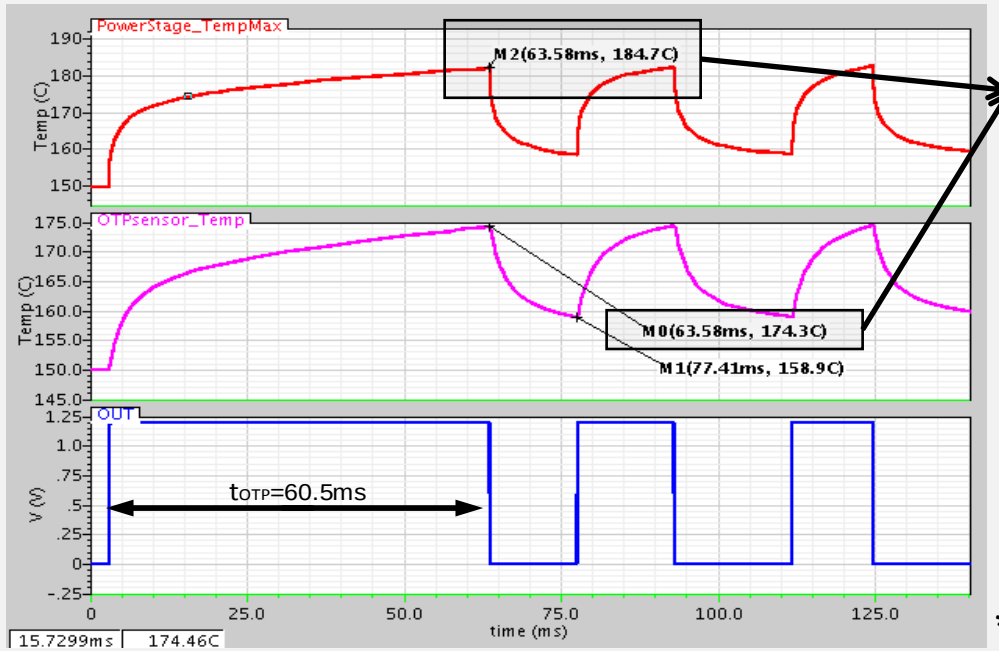
➢ Step 3: Electro-Thermal sims



Scenario



Electro-Thermal Sims



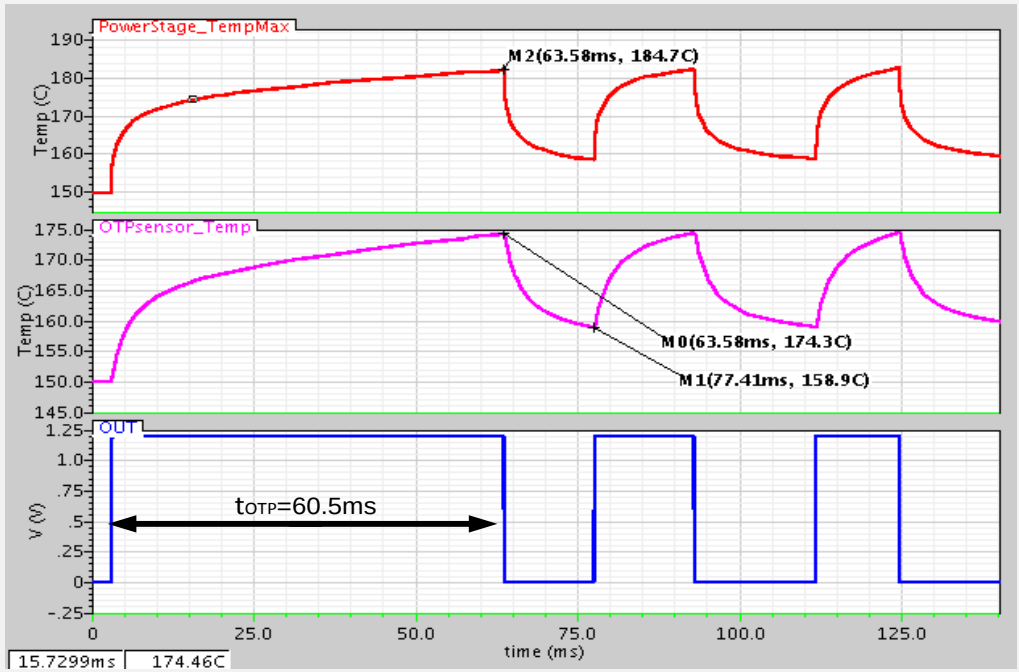
DeltaT=10°C

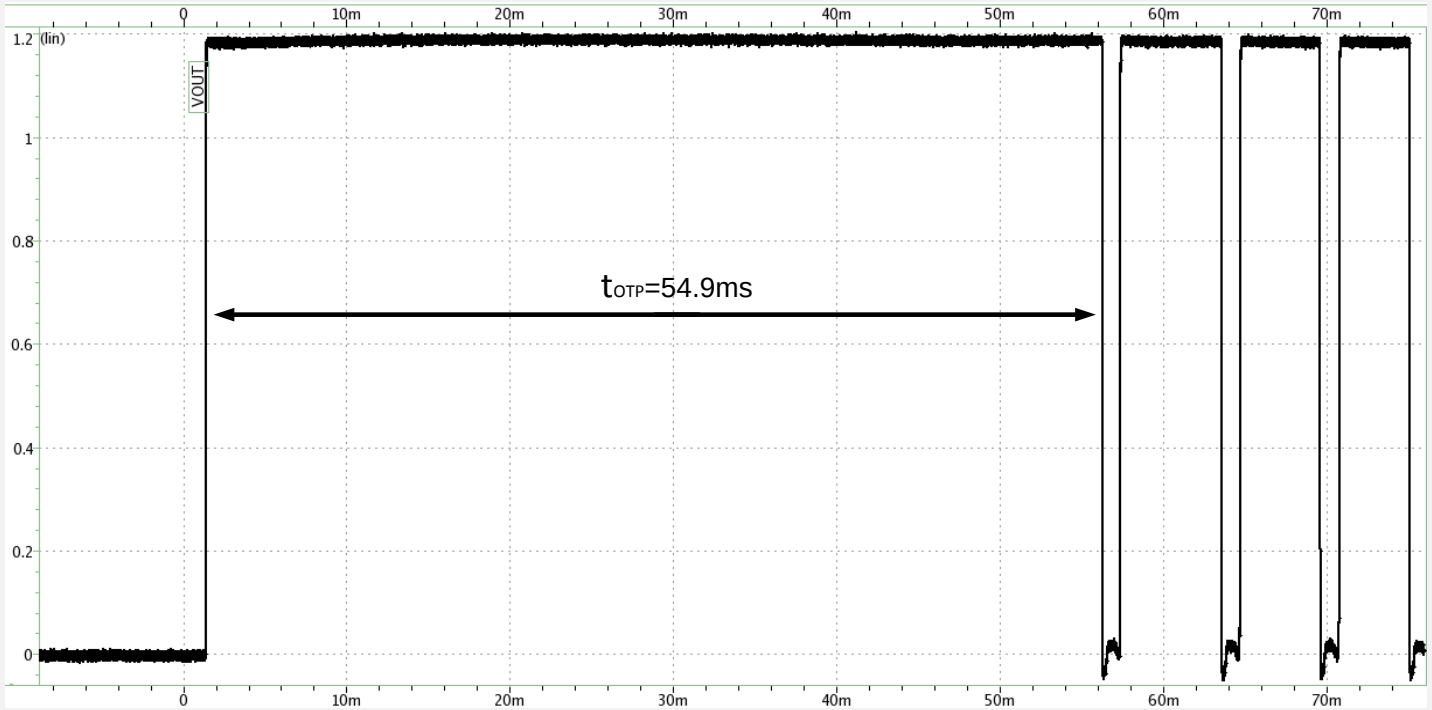
*coupled electro-thermal phenomena

*PAPPLIED=1.8W

Over-temperature protection: design methodology based on electro-thermal sims

- Measurement results:





- Good agreement between the measurements and the electro-thermal simulations results regarding the time until the OTP event occurs (t_{OTP}): 59.5 ms and 60.5 ms

Summary and Conclusions

- ***Systematic design (as opposed to simulation driven design):***
  - mathematical analysis => understanding of design constraints and trade-offs
  - sizing strategy => 1st iteration "design-by-hand" close-to-spec & help next iteration(s)
  - Optimization tools used only after a few "design-by-hand" iterations & driven by designer
- ***Analog designers need new tools and design methodologies***
  - Electro-thermal simulators crucial for robust design
  - Mechanical phenomena should also be considered, especially for duty-cycled operation
- ***Circuit design should be an important part of the development strategy for microelectronics***
  - Key part of the eco-system, essential for taking full advantage of new technologies
  - Experience & talent are essential in IC design => relocating jobs less likely than in software development
  - Easier to start-up and to scale-up successful design teams than technology-focused research
  - Romanian Universities have experienced teachers, as well as the design tools and access to silicon fabs. the students need in order to acquire the skills and abilities essential for IC design