The growing family of electrostatically-doped devices

Sorin Cristoloveanu, IMEP-LAHC Minatec, Grenoble, France

Outline

- Concept

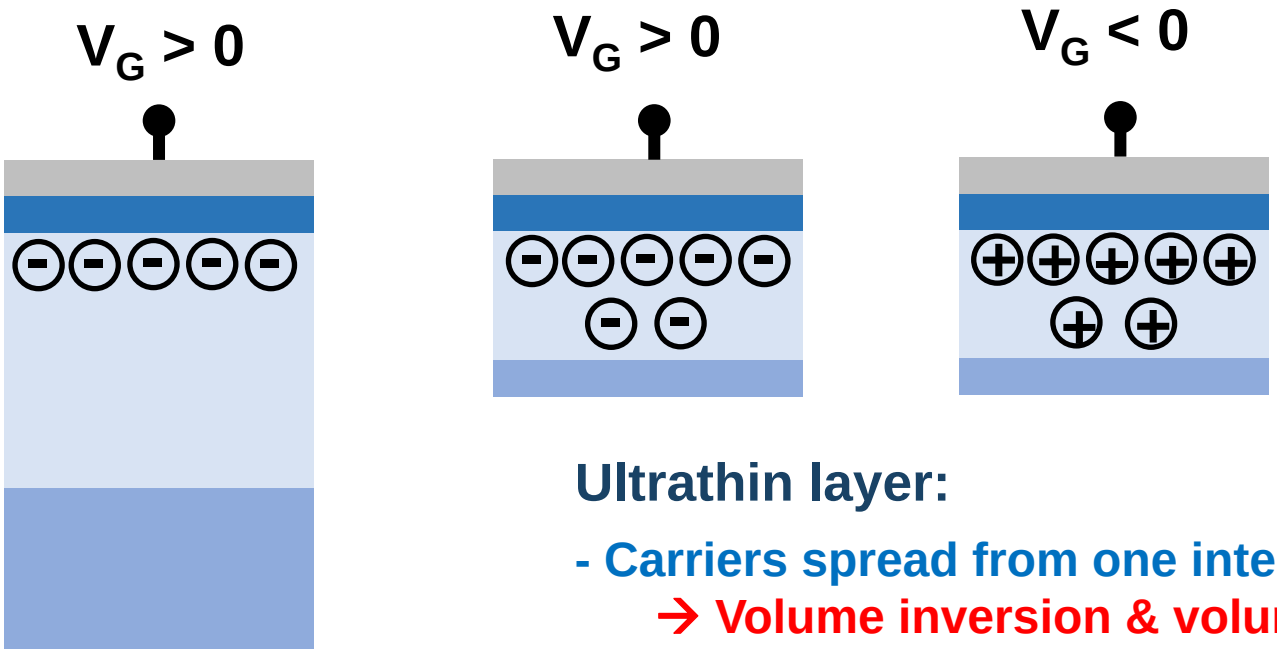
- Typical applications in NWs and 2D materials

- The Hocus-Pocus diode

- Other FDSOI devices with electrostatic doping

- Conclusions

MOS Capacitor



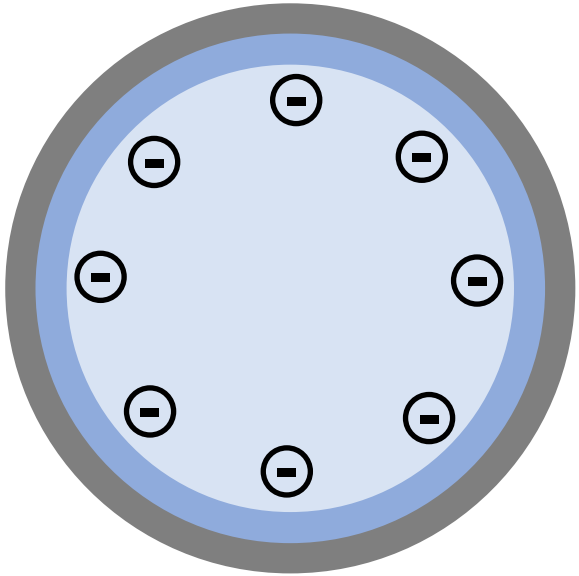
Ultrathin layer:

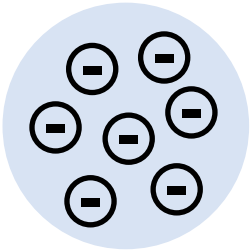
- Carriers spread from one interface to the other
  → Volume inversion & volume accumulation
- The whole film is filled with electrons or holes
- Kind of N & P doping: electrostatic

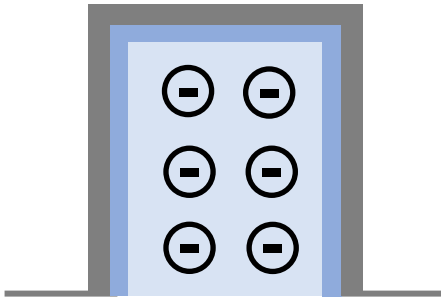
Bulk Si:

- Inversion layer at interface (2D)
- Depletion region
- Neutral substrate

Nanowires and FinFETs







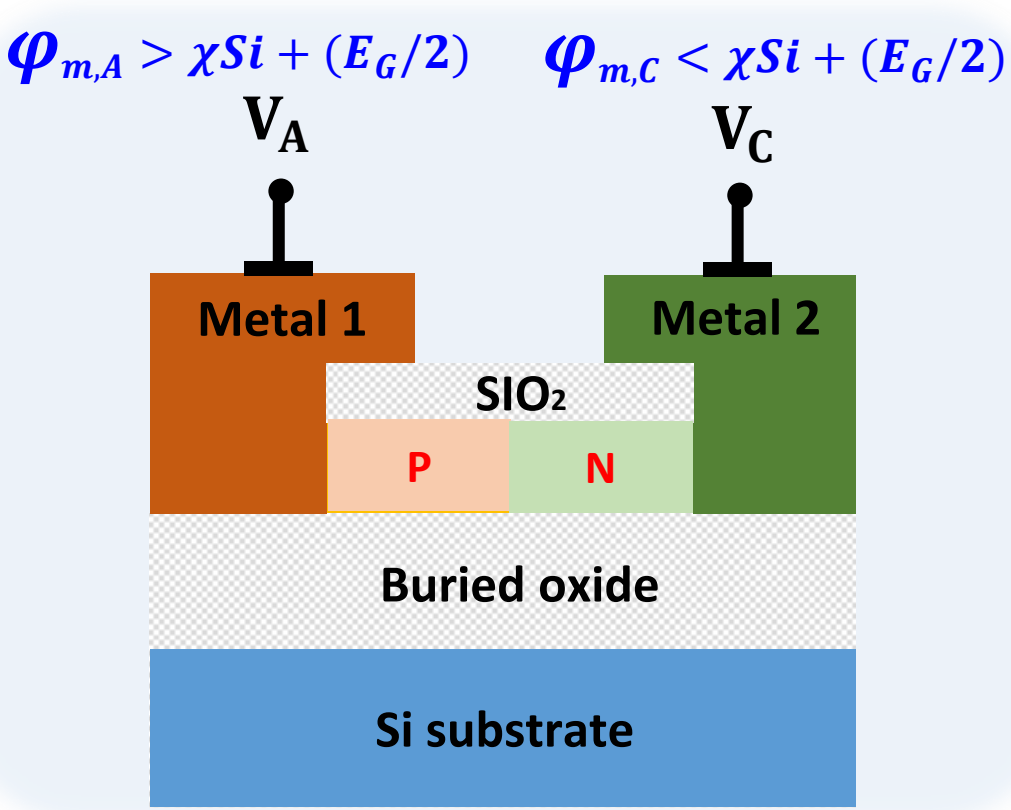
Thick NW:

- Inversion layer at interface
- Depletion region
- Neutral substrate

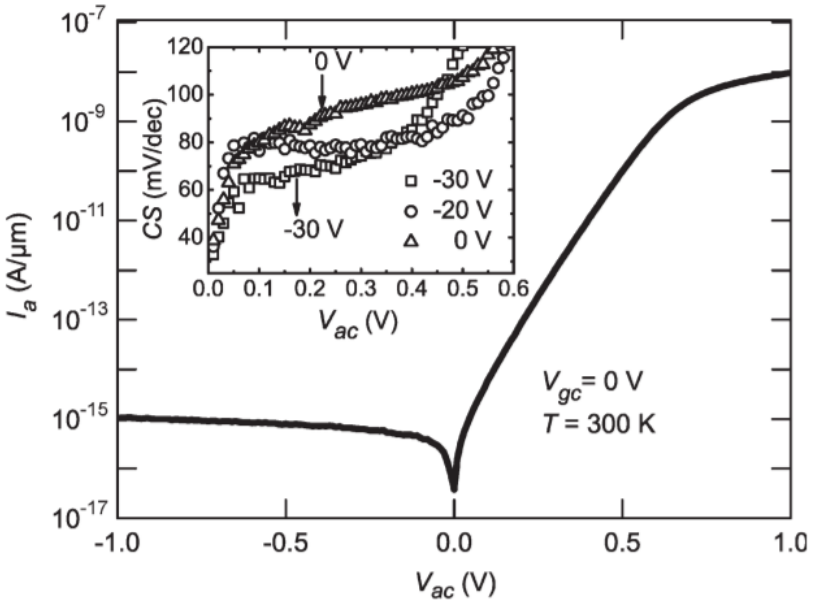
Thin NW or FinFET:

- Volume inversion/accumulation
- Electrostatic doping

Charge-Plasma Diode

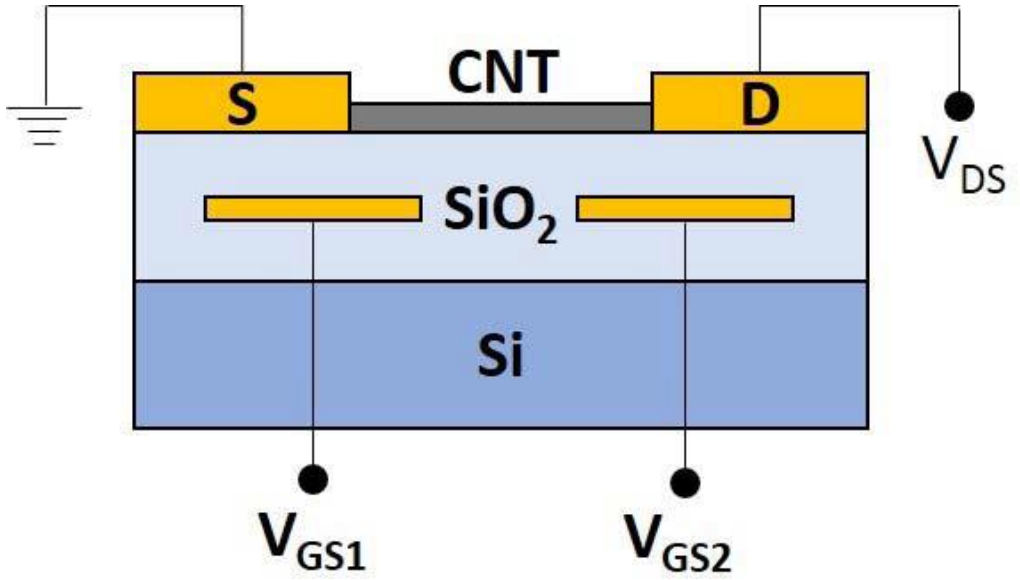


- Low-temperature budget
- No dopant implantation



Hueting, R. J., et al. "The charge plasma pn diode," *Electron Device Letts.*, 2008

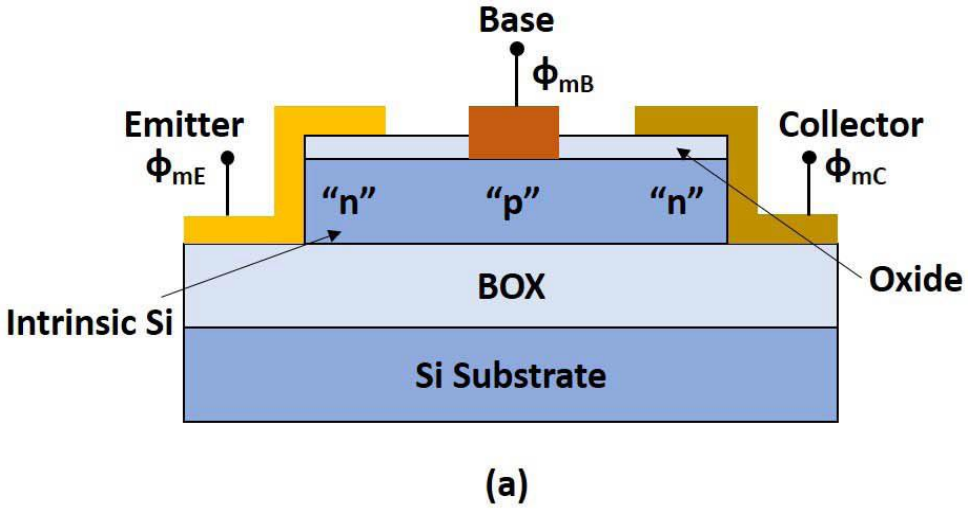
Carbon Nanotube Electrostatic Diode

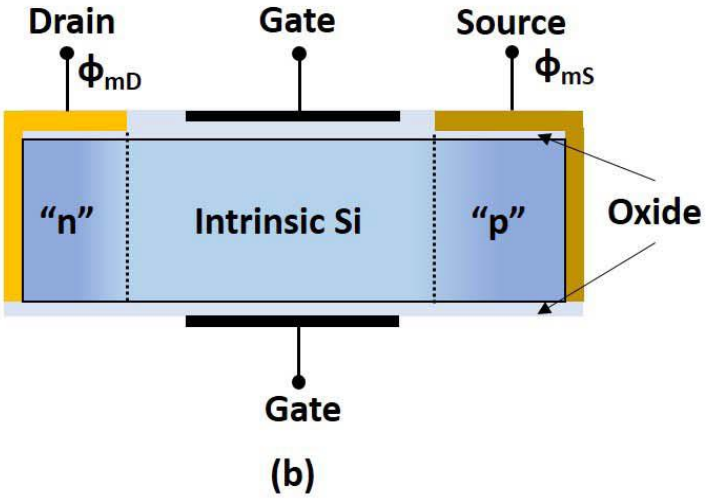


- Split MOS gates for reconfigurable device
- Gates with opposed polarities → electrostatic diode
- Gates with same polarity → N-channel or P-channel transistors
- The electrostatic P-N junction is not abrupt (inter-gate gap)

[Lee et al, APL 2004]

Other Charge-Plasma Devices





Lateral Bipolar Transistor

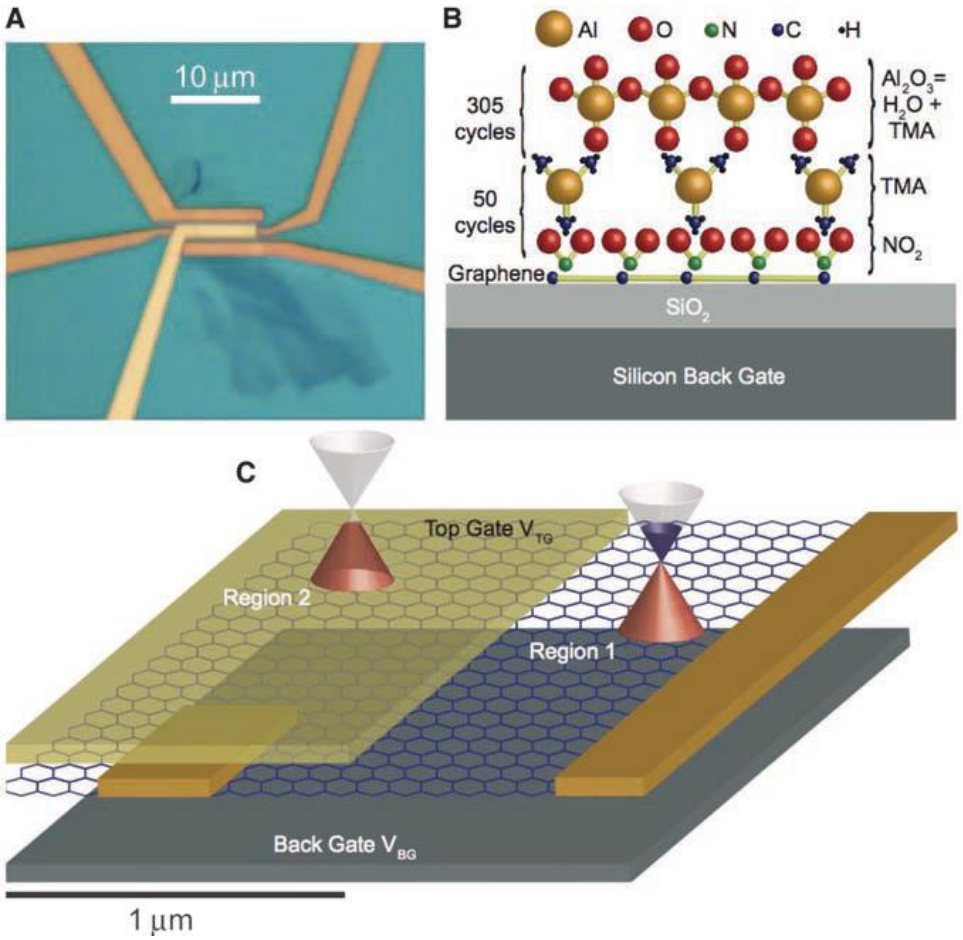
- 3 different metal workfunctions

Tunneling FET

- MOS gate added

[Gupta et al, TED 2017]

Electrostatic Diode on Graphene

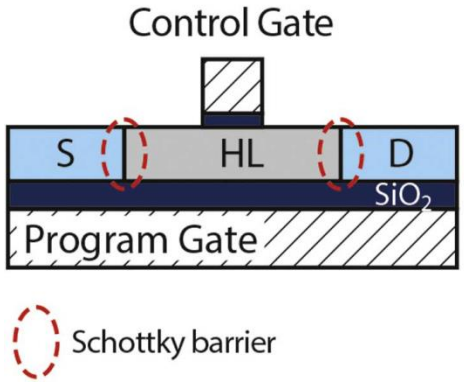


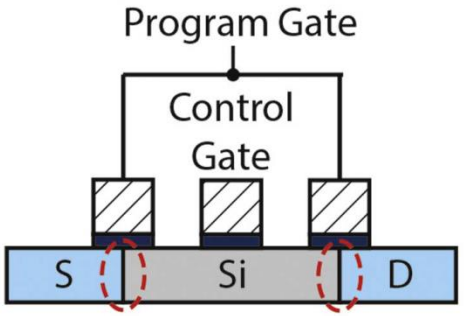
- Front and back MOS gates
- Electrostatic P-N junction
- Used for quantum Hall effect

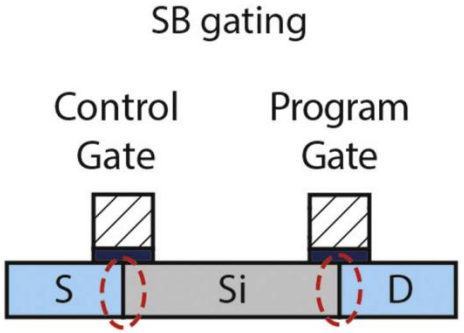
[Williams et al, Science 2007]

Reconfigurable NWs

Back gate & Top gate | **3 top gates** | **2 top gates**

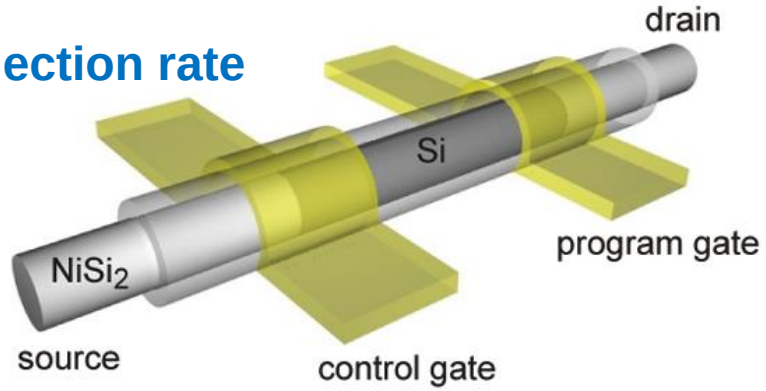


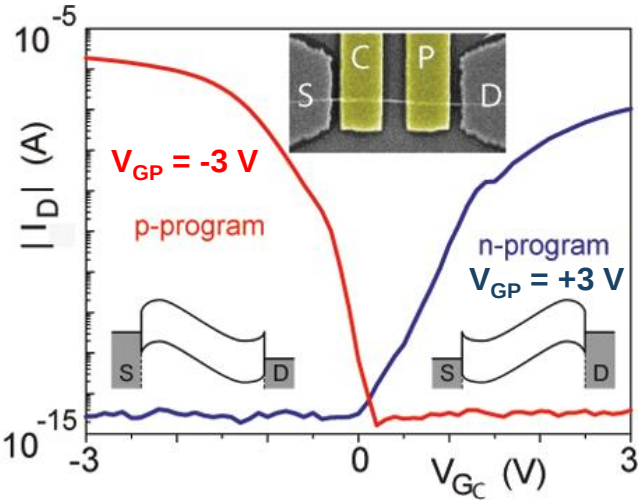




[Mikolajik et al,SST 2017]

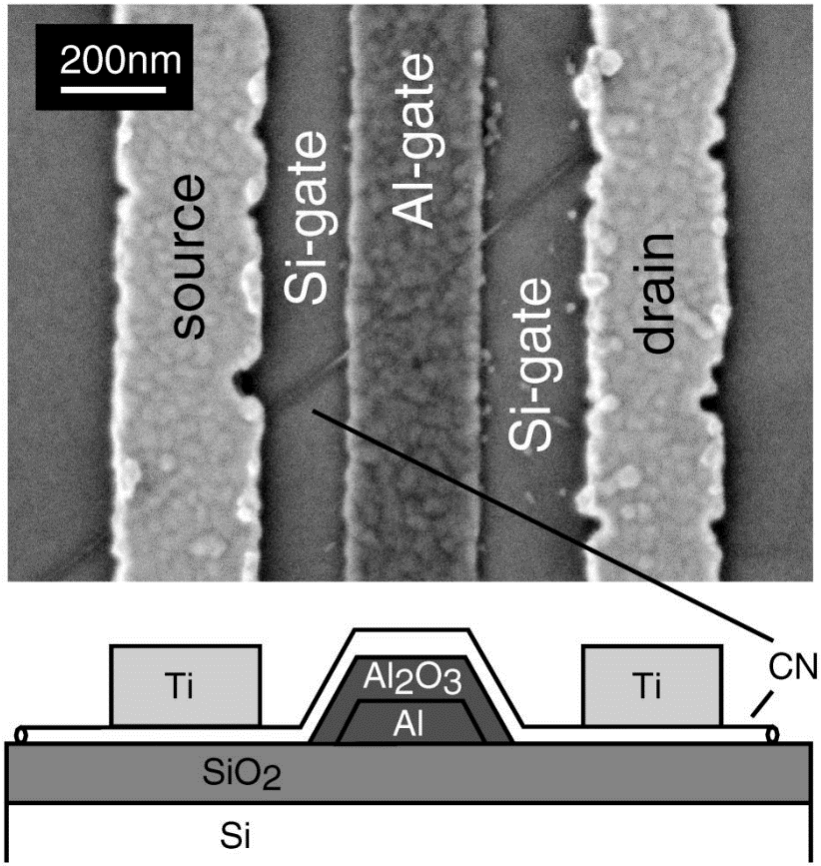
- Program gate → N or P-FET
- Control gate → injection rate





[Heinzig et al, NANO Lett 2012]

Carbon Nanotube FET with BTBT



- Back gate (Si) defines S/D doping
- Al gate controls drain current
- BTB tunneling at P+/N+ junctions

[Appenzeller et al, PRL vol 93 2004]

Why Electrostatic Doping?

- Necessity in 2D materials, CNT, some vertical nanowires
  - How to make source/drain contacts without ion implantation?

- Natural benefit of ultrathin body technologies
  - Conceive innovative devices: useful and reconfigurable
  - FinFETs & GAA nanowires – top gate action
  - FDSOI – top and back independent gates
    – more options and flexibility

Ultrathin LDMOS

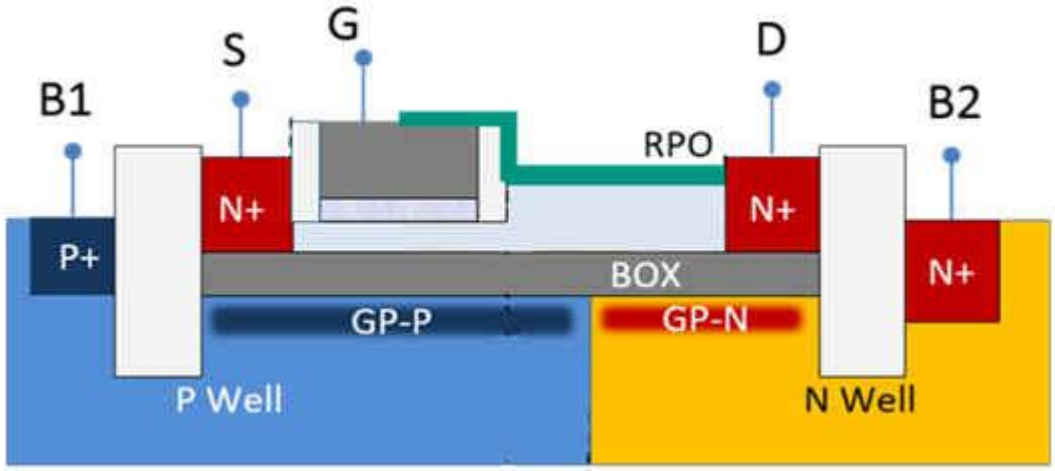
High-voltage (5 V) devices needed for power management

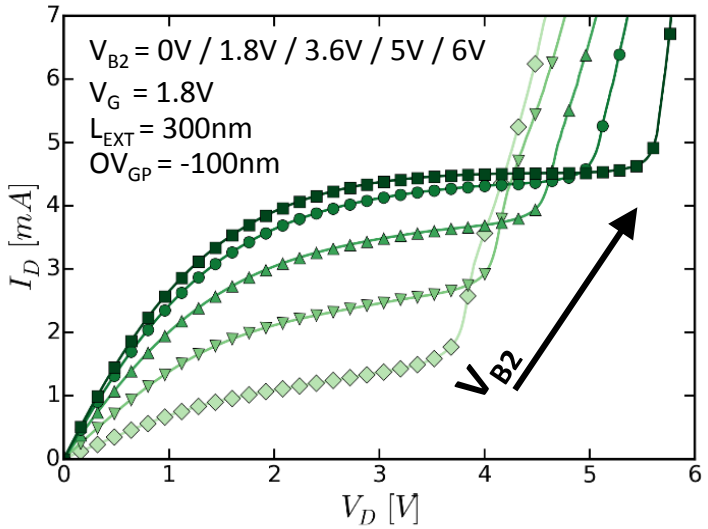
In FD-SOI, the drift region should not be fully depleted!

Doping required: implanted or electrostatic?

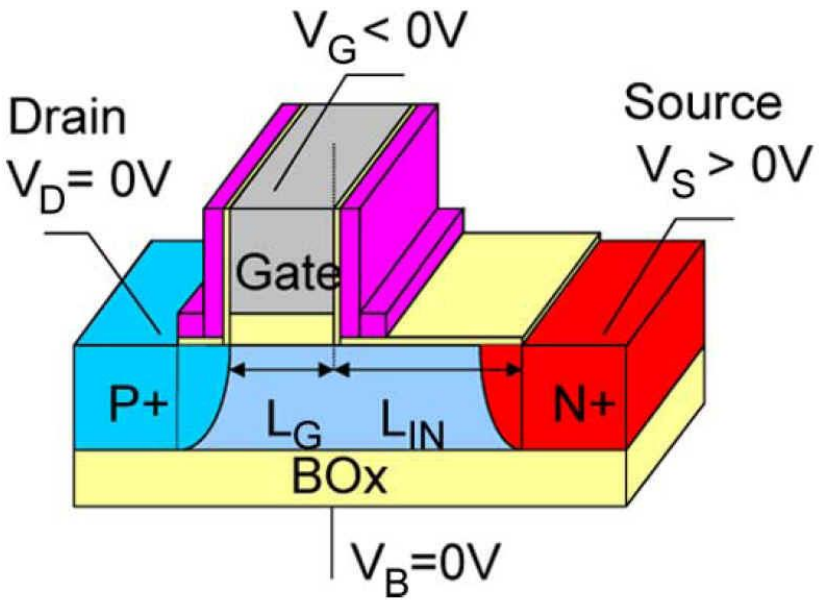
Dual ground-plane EDMOS

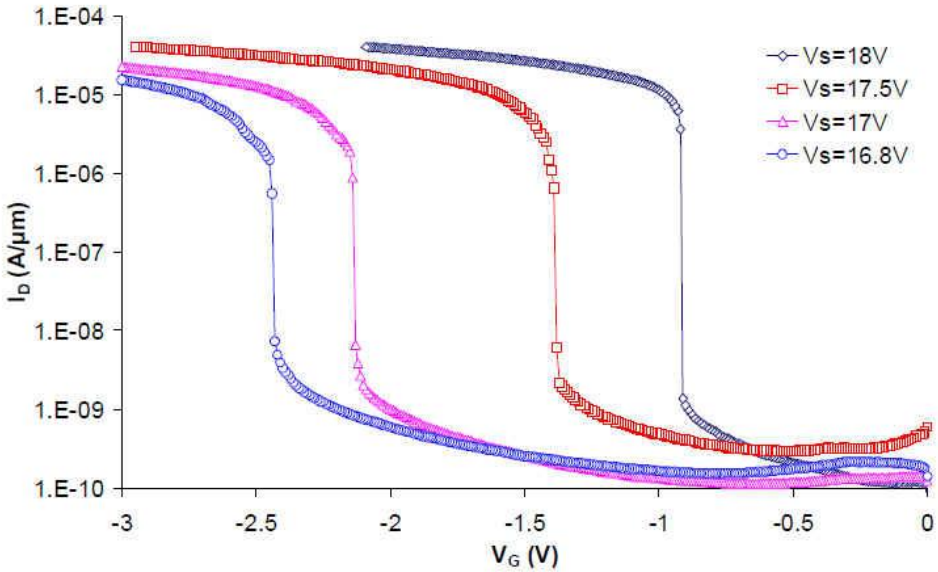
- From conventional single-gate LDMOS to triple-gate in FD-SOI
- GP-N controls the doping in drift-region and GP-P the MOSFET V_T





I-MOS: Impact Ionization MOSFET



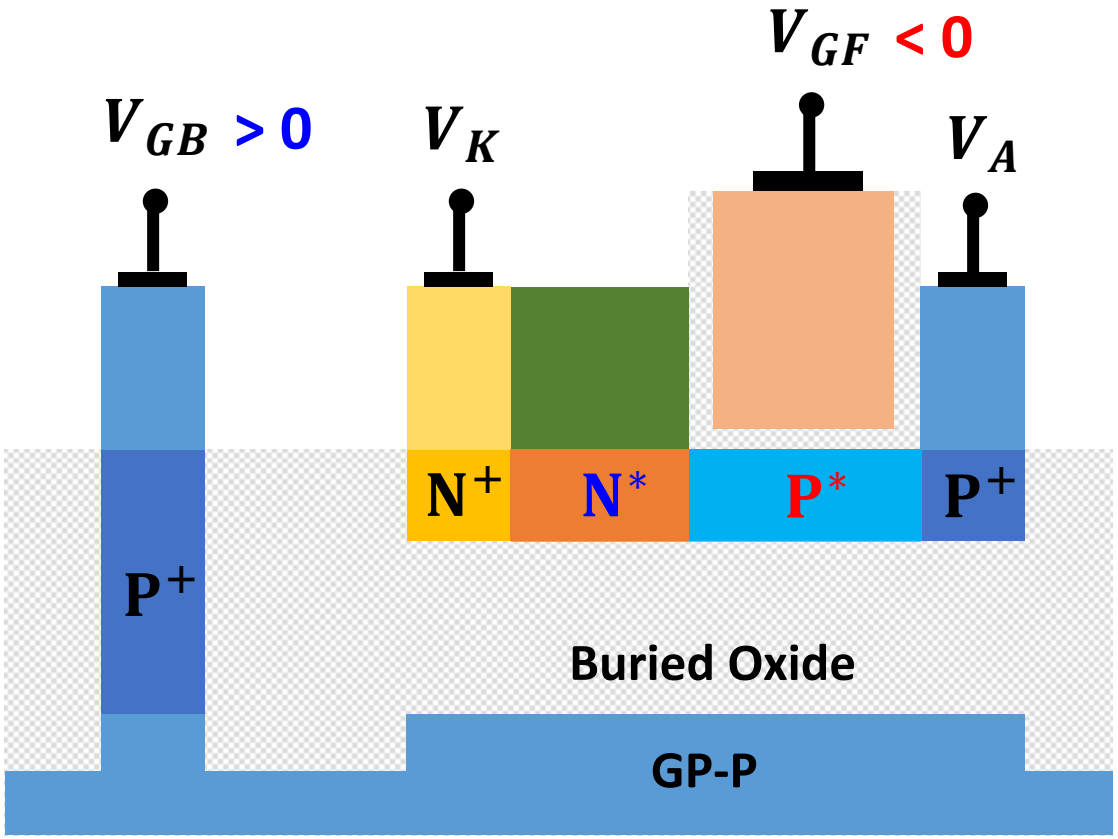


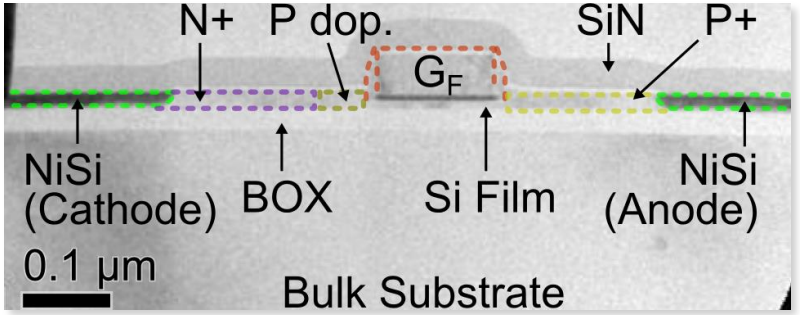
- **Reverse-biased PIN diode – For $V_G = 0$: off-state**
- **For $V_G < 0$ (on-state): Hole accumulation virtually extends P^+ contact under the gate**

  → shorter diode → higher electric field → impact ionization → avalanche breakdown
- **Excellent swing: *S* = 2 mV/decade**
- **Terrible V_S voltage: ~ 18 V**

[Mayer et al, 2006]

Hocus Pocus Device





Fabricated at ST Microelectronics

Hocus Pocus Diode Configurations

(A)

(B)

(C)

$V_{GB} > 0$

(D)

(E)

(F)

$V_{GB} = 0$

(G)

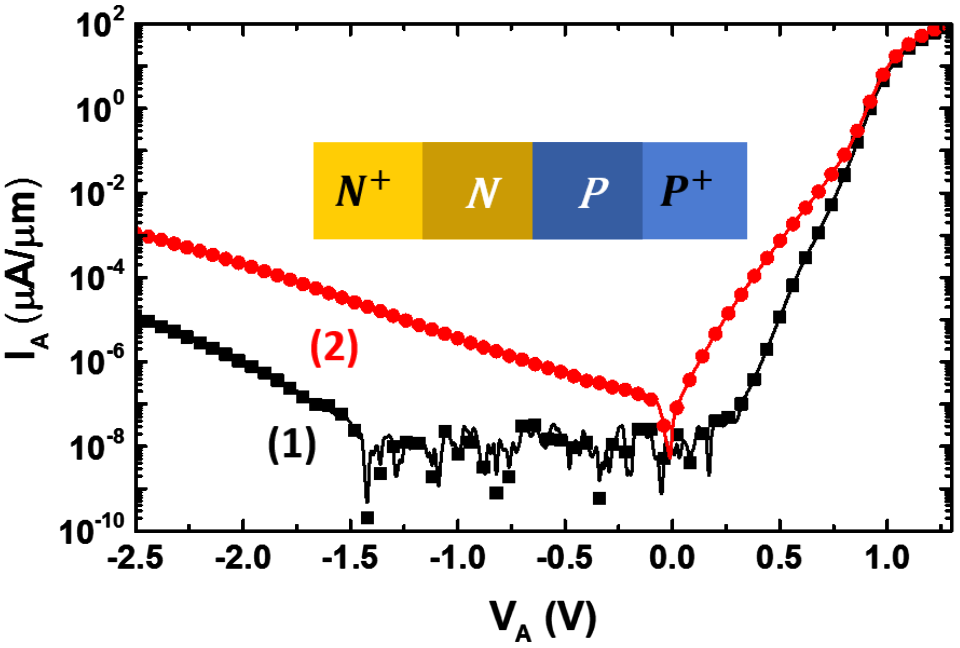
(H)

(I)

$V_{GB} < 0$

$V_{GF} < 0$ $V_{GF} = 0$ $V_{GF} > 0$

The Virtual Diode: Characteristics

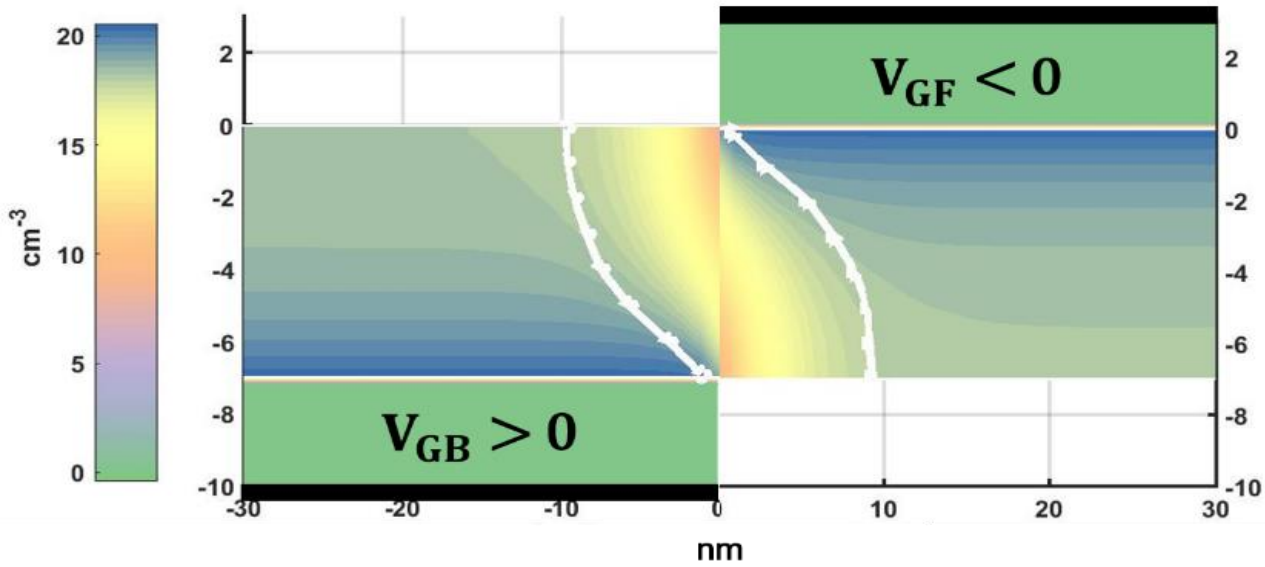


(1) $V_{GF} = -1.2\ V, V_{GB} = +5\ V$

(2) $V_{GF} = -2\ V, V_{GB} = +10\ V$

- I-V characteristics as in a physical diode
- The reverse current is extremely low ($10^{-8}\ \mu A/\mu m$)
- ON/OFF ratio ~ 10^{10}
- Doping can be increased at demand

Simulation : Virtual diode



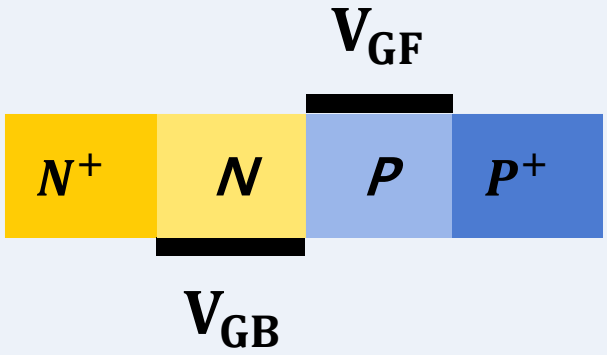
- Gate action leads to a 2D effect
- In-depth variation of depletion width and barrier height
- Defined by the concentrations of free carriers
- The concentration of ionized acceptors is low and identical on both sides of the P-N junction

Electrostatic diode *vs.* standard diode

Physically-doped diode

- Constant doping
- Symmetrical characteristics
- Simple 1D P-N diode model

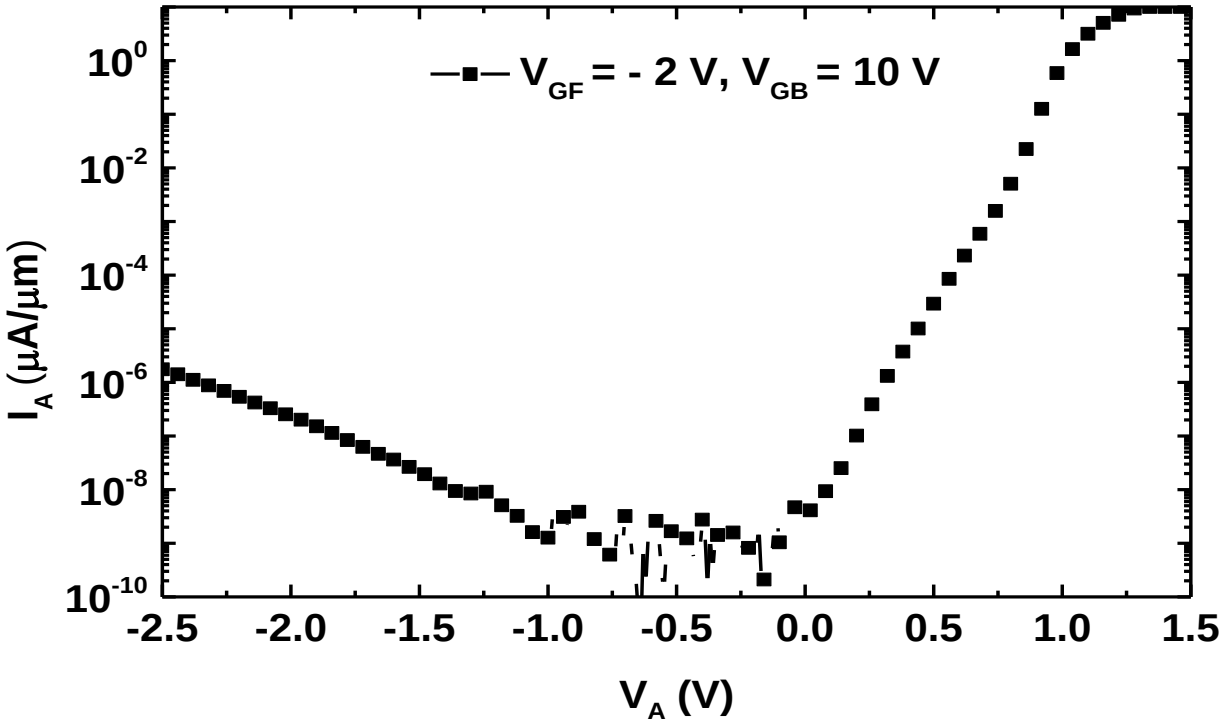
Virtual electrostatic diode



- Virtual doping is tunable by gates
- Dynamic change in carrier concentrations with V_A
- Asymmetrical characteristics
- Space charge region: 2D effect
- Highly reconfigurable P-N junction

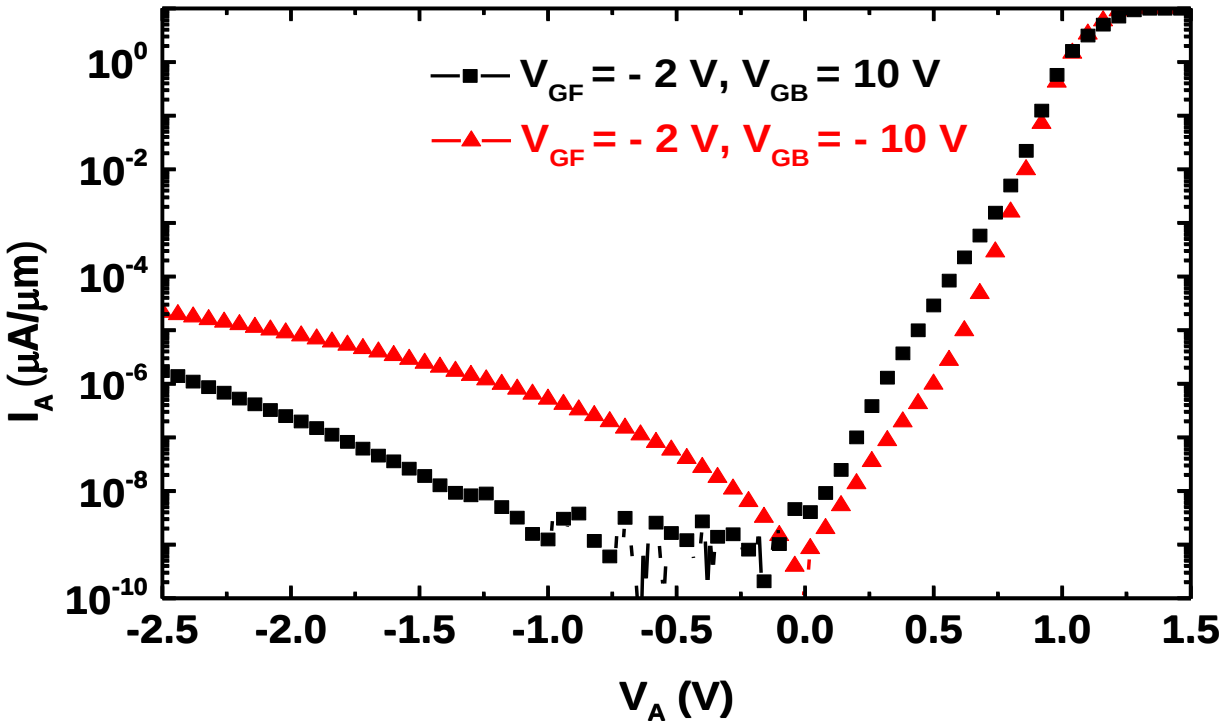
Metamorphosis of Hocus-Pocus diode

Full Virtual Diode



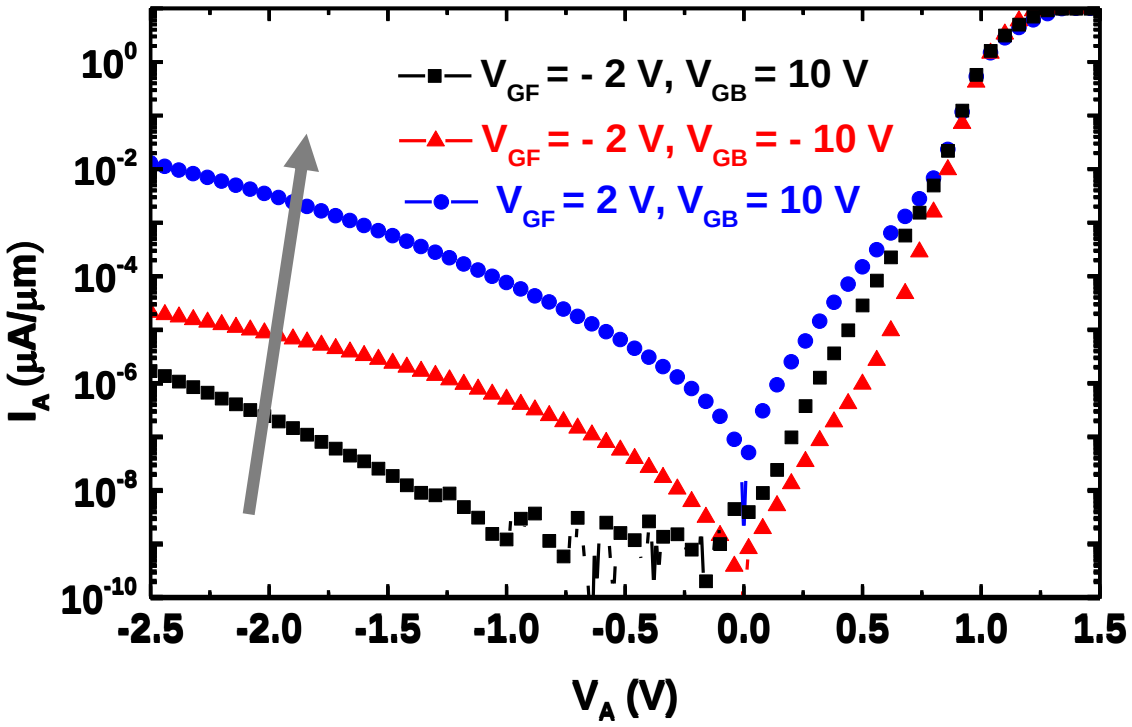
Semi-virtual Diode

Left-sided Junction Diode



Semi-virtual Diode

Right-sided Junction Diode



Higher Reverse Current

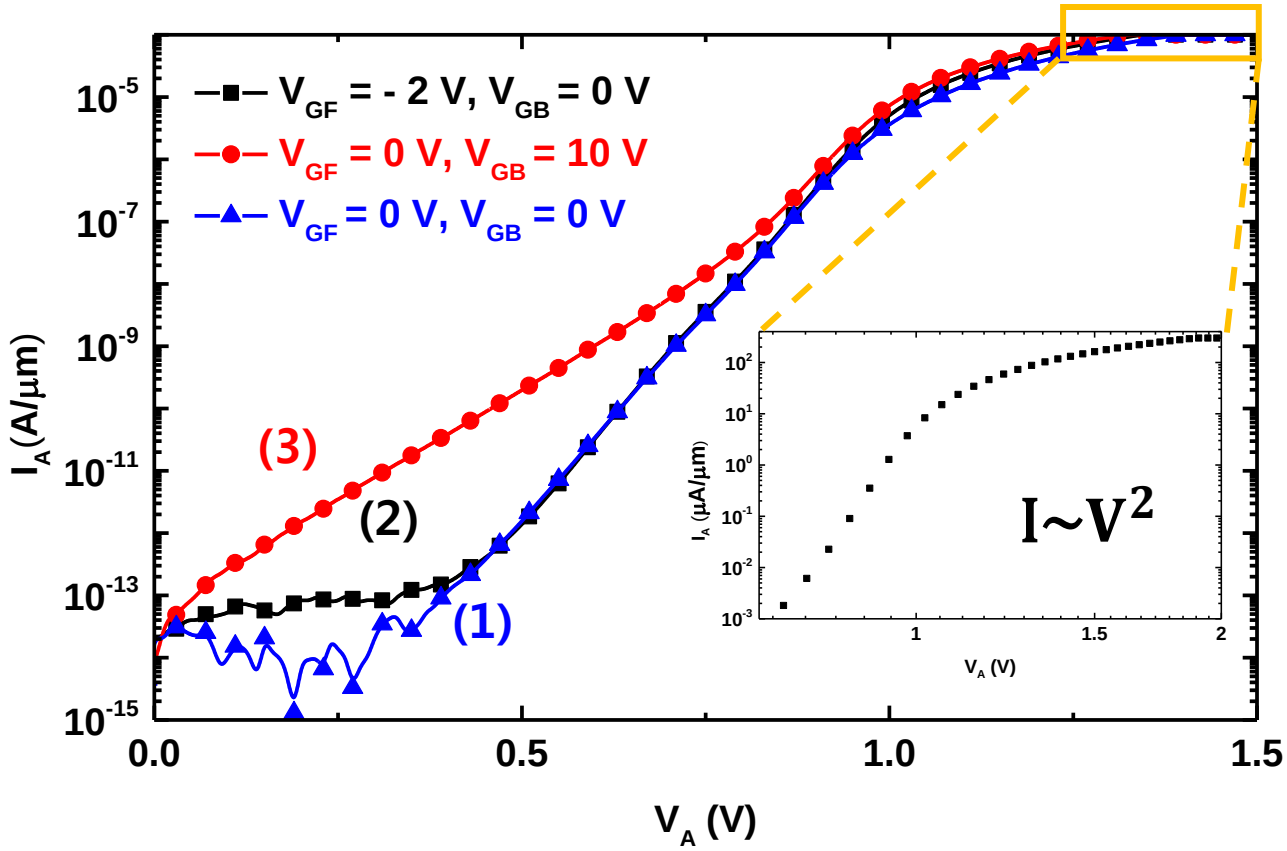
- BTBT at the junction
- Higher BTBT rate at the P^+ terminal
- Stronger front-gate action

Metamorphosis: Several PIN diodes

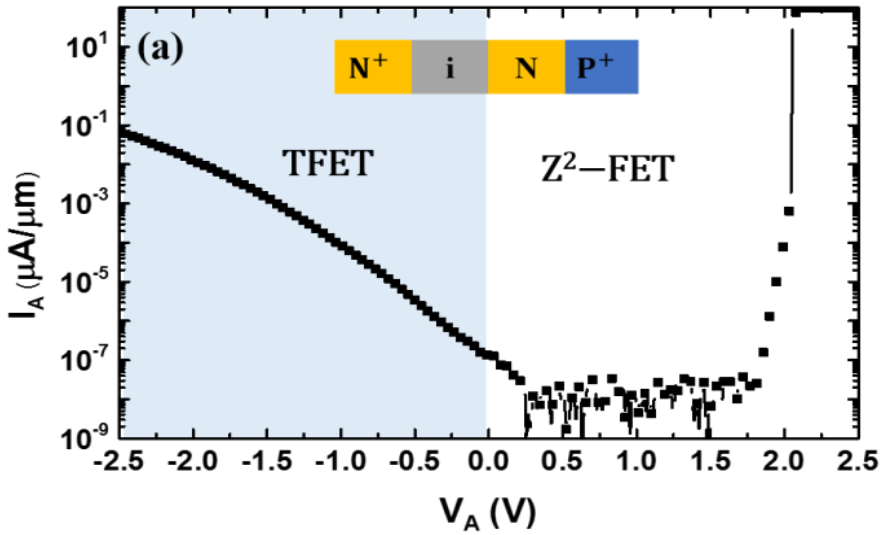
(1) Full-bodied Diode

(2) Half-bodied Diode

(3) Half-bodied Diode



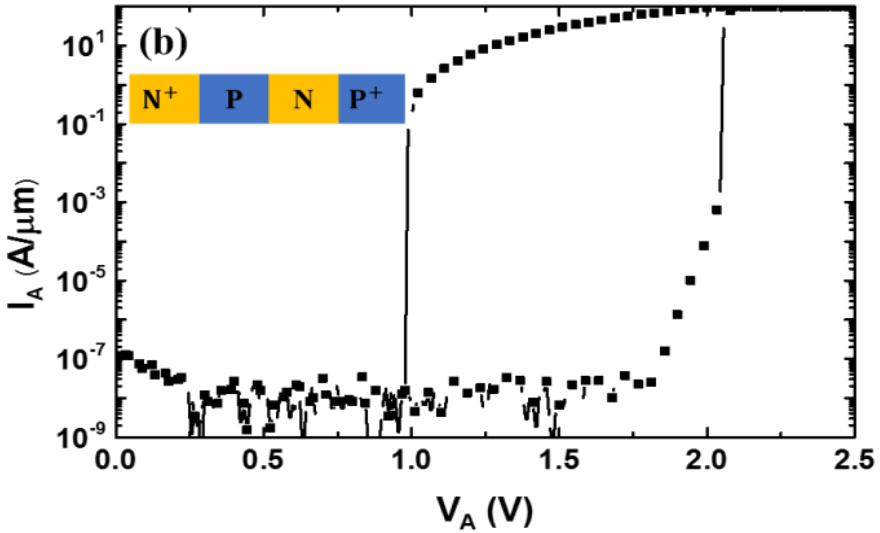
Metamorphosis: TFET and Z²-FET



Reverse bias → TFET

Forward bias → Z²-FET

(band-modulation device)

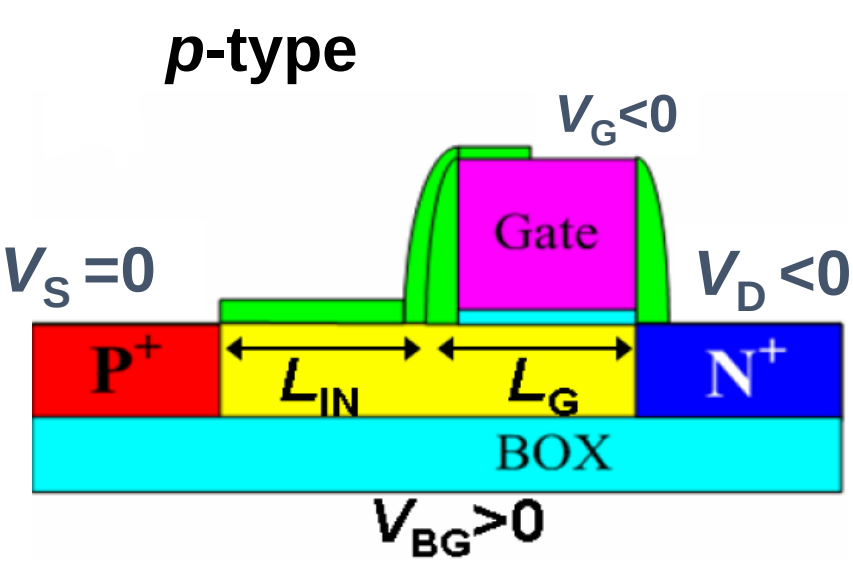


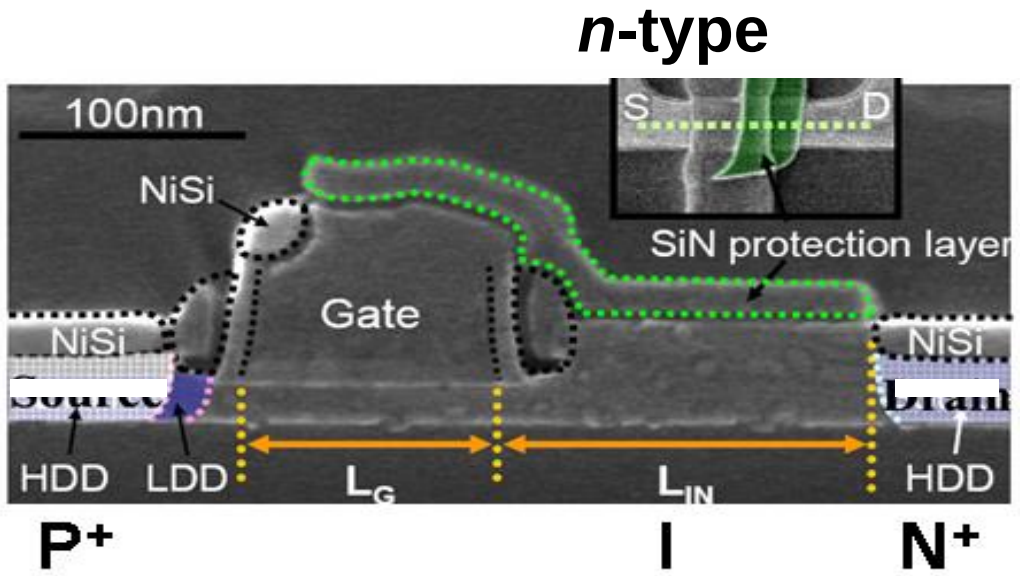
Improved Z²-FET

(virtual thyristor)

Metamorphosis of Hocus-Pocus diode in Z^2-FET

A Sharp Switching Device: Z²-FET





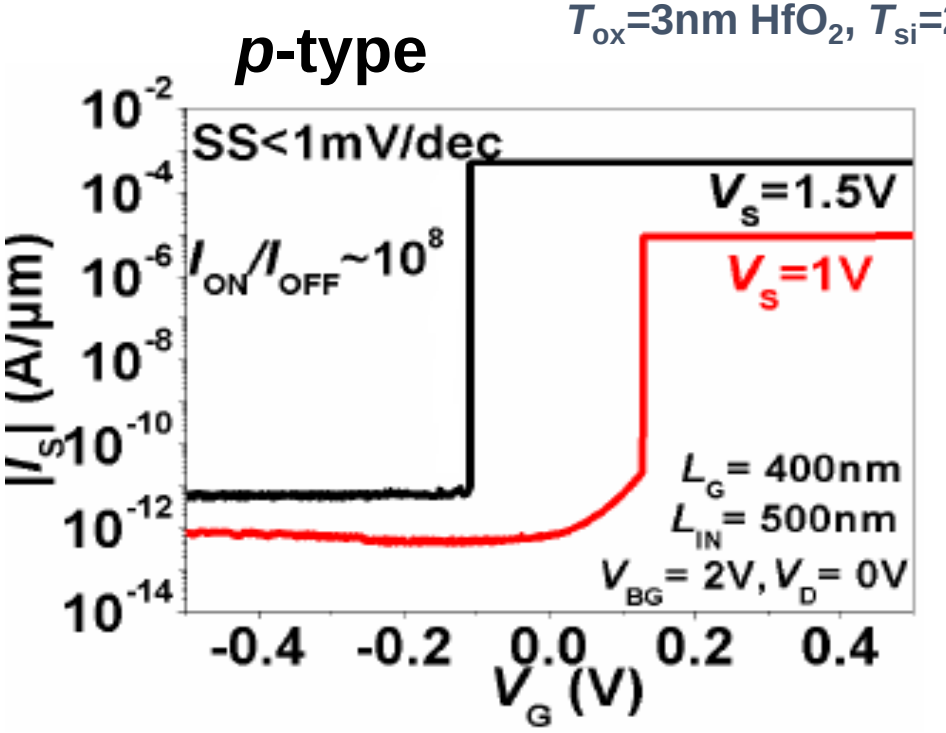
Thyristor-like **virtual** junctions

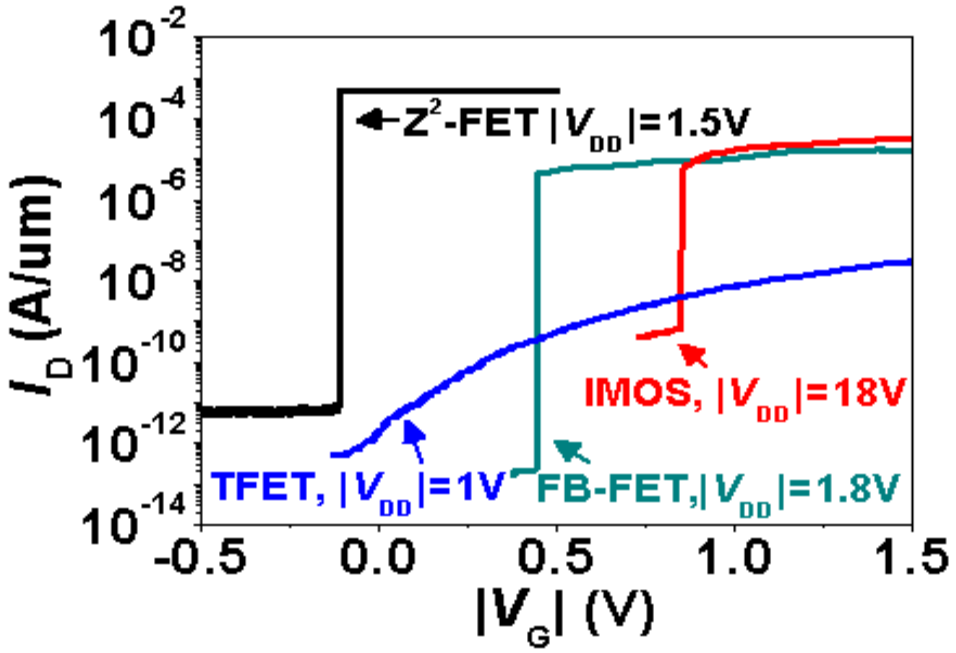
Z²-FET: Zero subthreshold swing and Zero impact ionization FET

- Forward-biased gated PIN diode, undoped channel
- Front-gate bias V_G and back gate bias V_{BG} used to emulate N & P regions
- Fabrication-compatible with SOI CMOS

Z²-FET: I_D–V_G Characteristics

T_{ox}=3nm HfO_2, T_{si}=20nm, T_{BOX}=140nm [Wan, Sorin, Alex, Cyrille]



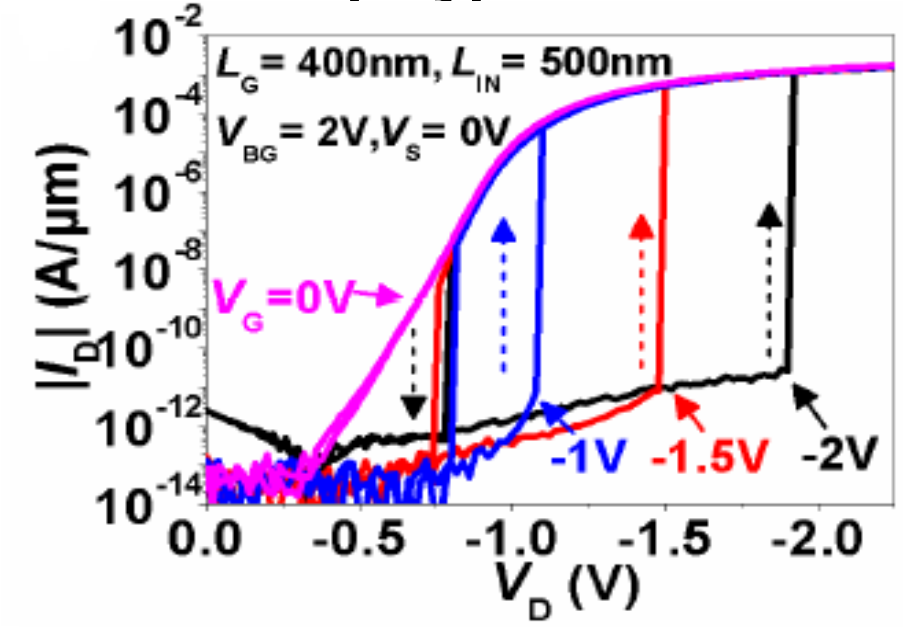


- I_{ON}/I_{OFF} >10^8 and Swing < 1mV/dec
- V_{th} is tunable by the drain bias
- Outperforms FB-FET, TFET and IMOS

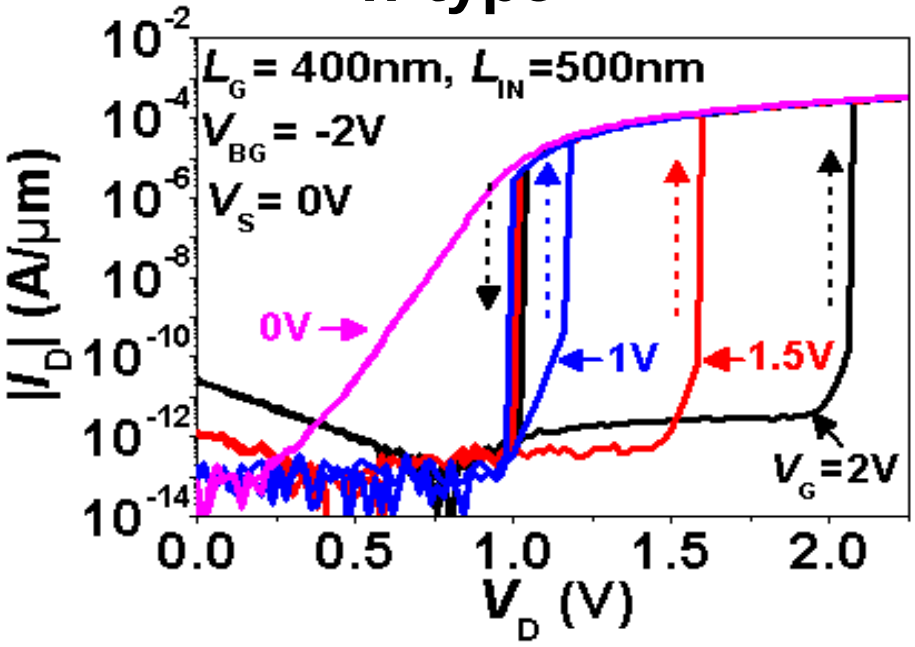
IMOS: F. Mayer et al., ESSDERC, 2006.
TFET: F. Mayer et al., IEDM, 2008.
FB-FET: A. Padilla et al., IEDM, 2008

Z²-FET: I_D–V_D Characteristics

p-type

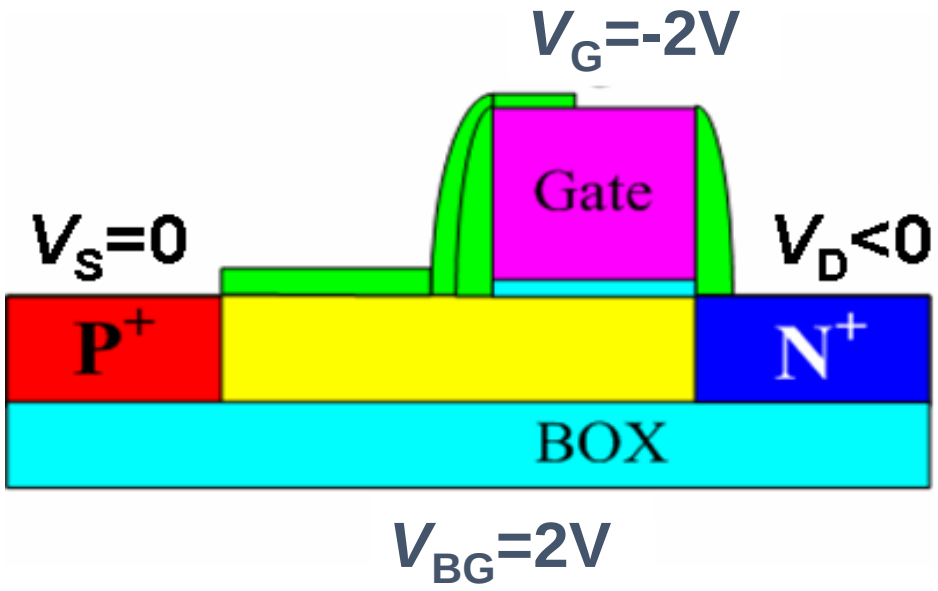


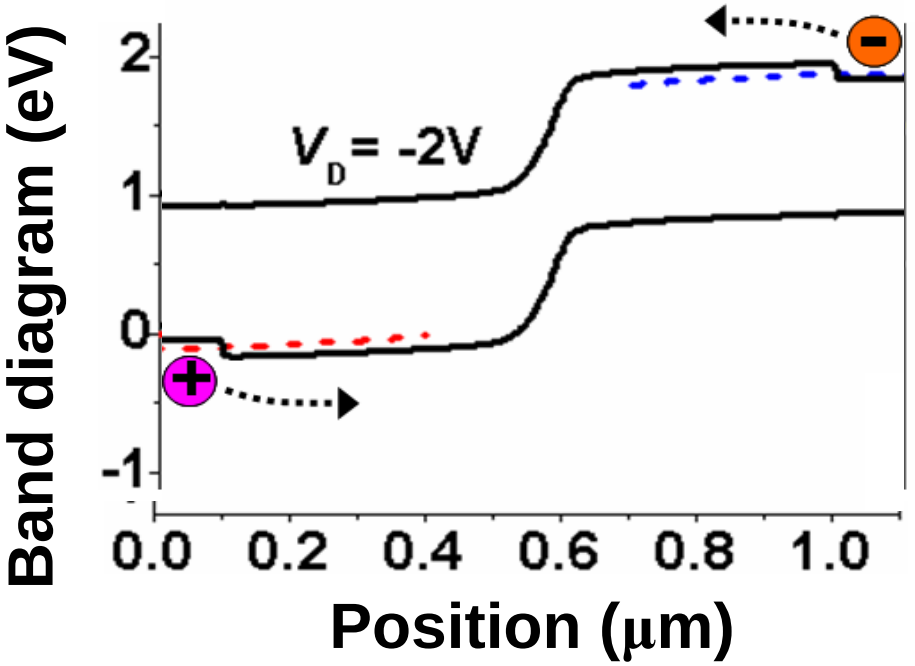
n-type



- Sharp switch at $V_D = V_{ON}$
- Hysteresis between forward and backward sweep
- V_{ON} depends on V_G → memory application [J. Wan et al., IEEE EDL 2012]
- Both *n*-type and *p*-type devices work well

Z^2-FET: Operation Principles





TCAD Simulations:

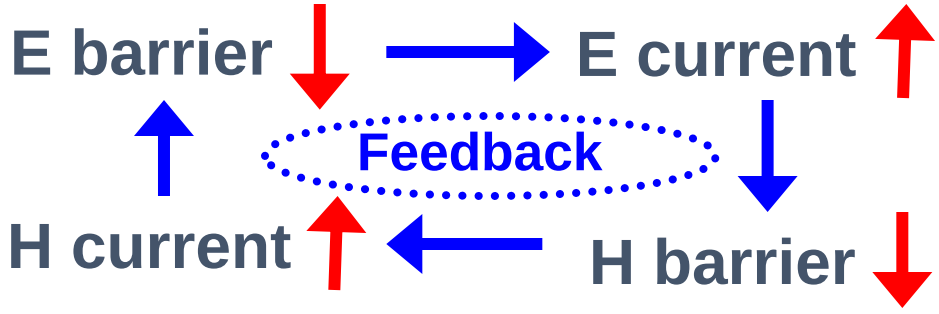
Reproducing experiments:

sharp switching + hysteresis

Impact ionization not involved

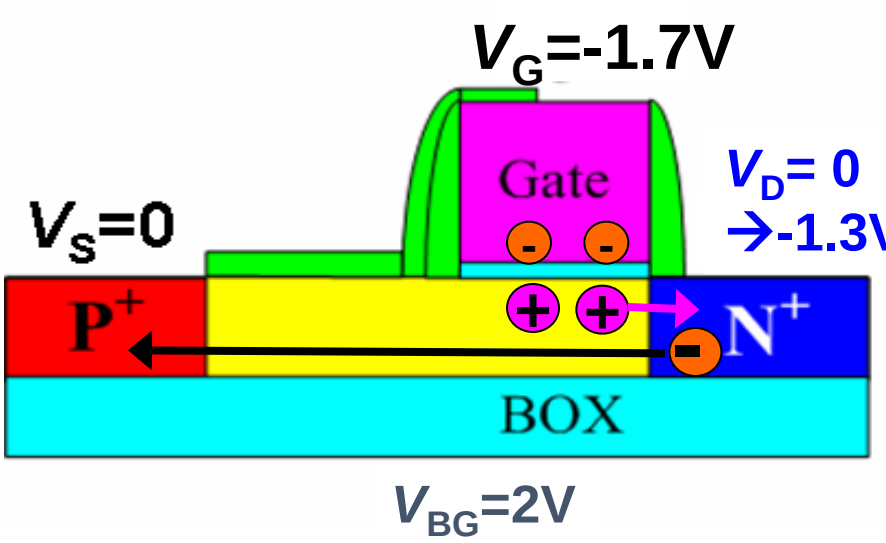
Z^2-FET variants: surface charge [Padilla]

two gates [Ioannou et al]

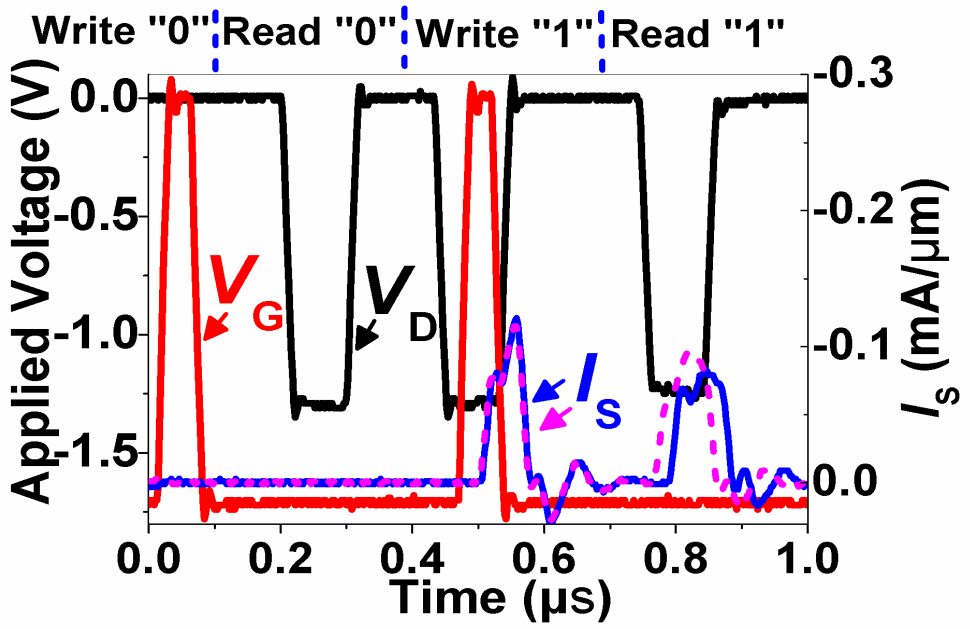


Z^2-FET:
Applications

Z²-FET: High Speed 1T-DRAM



[J. Wan et al., IEEE EDL 2012]

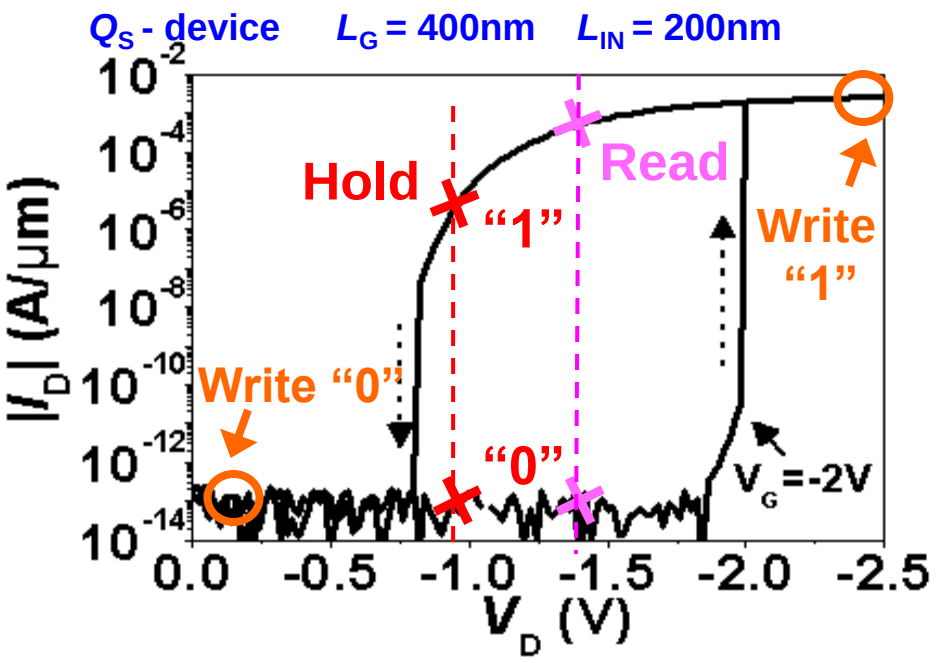


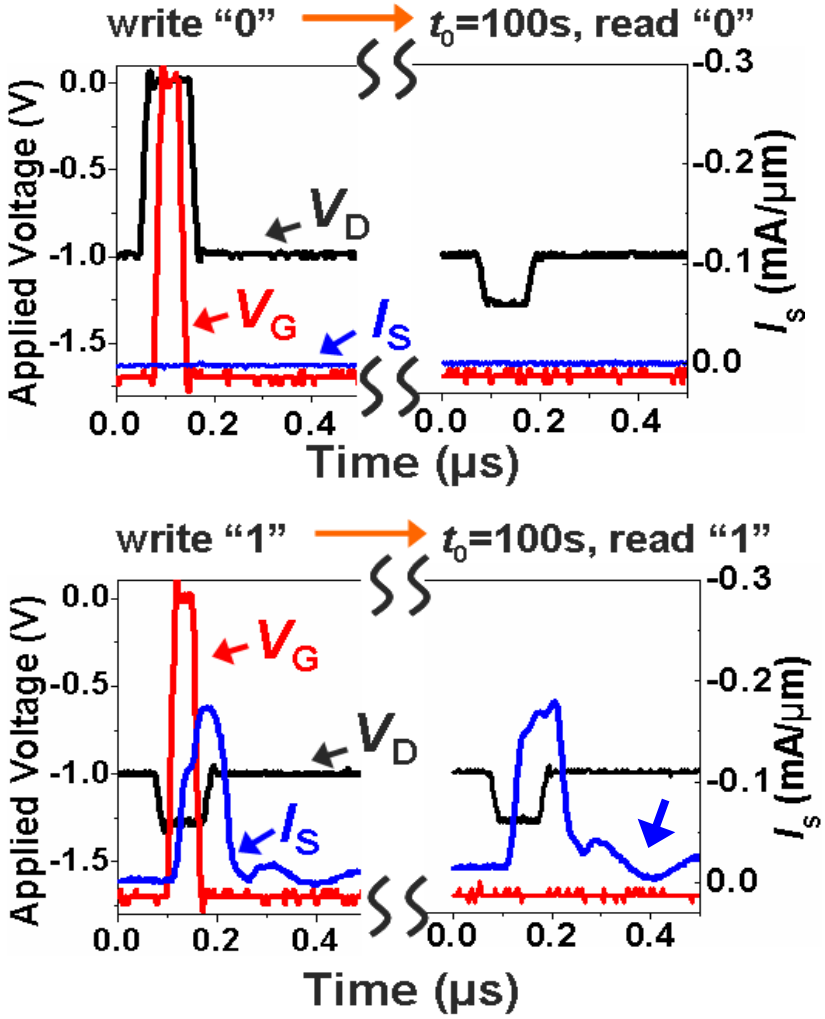
- Capacitor-less, compatible with SOI CMOS fabrication
- State '1' set by **small** charge on front-gate capacitor (C_G)
- V_D read pulses → discharge of C_G reduces E barrier → feedback & high I_S

☺ Low $|V_{DD}|$ ~ 1.1 V operation; Current sensing margin $I_1 / I_0 > 10^8$

☺ Simulated 1 ns access time, thanks to ***internal feedback*** $I_G = \Delta Q_G / \Delta t$ instead of ***external amplifier*** in 1T-1C DRAM

Z²-FET as 1-T SRAM



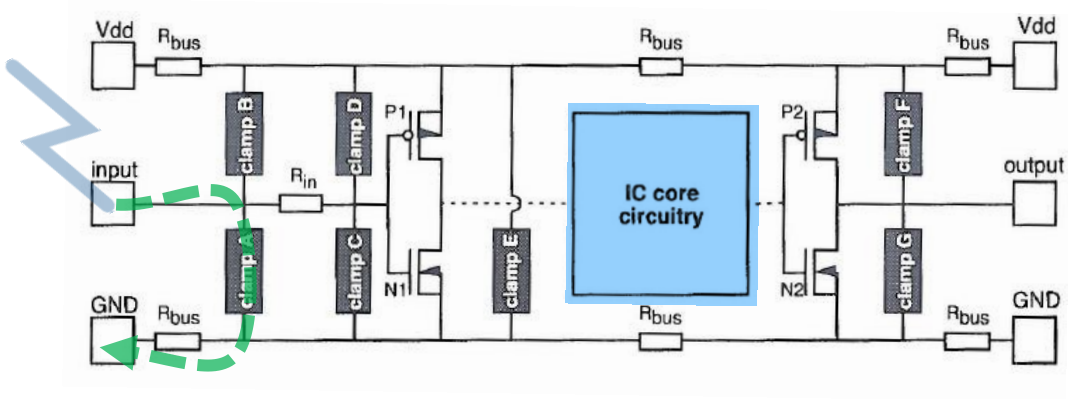


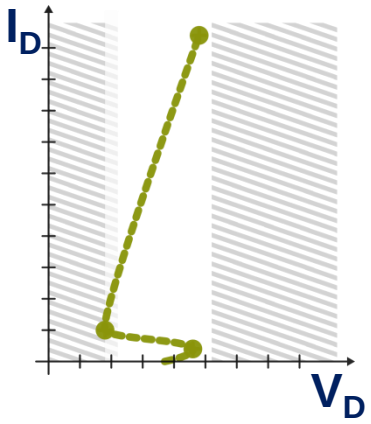
The hysteresis in I_D-V_D is directly used for SRAM operation

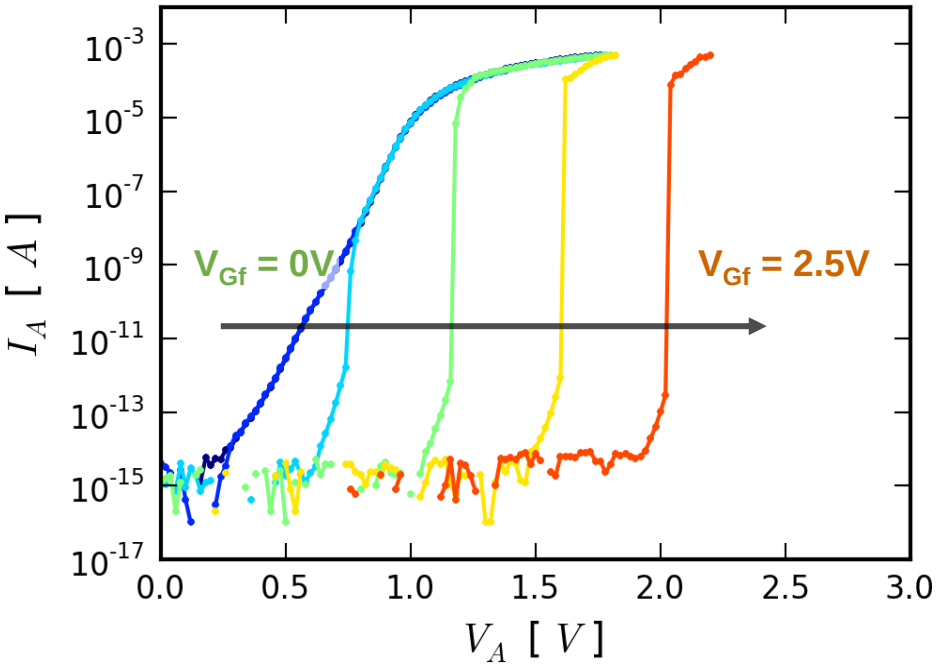
☺ Data needs no refreshing

☹ Static current and power consumption for holding logic "1" (can be reduced)

Z²-FET for ESD protection



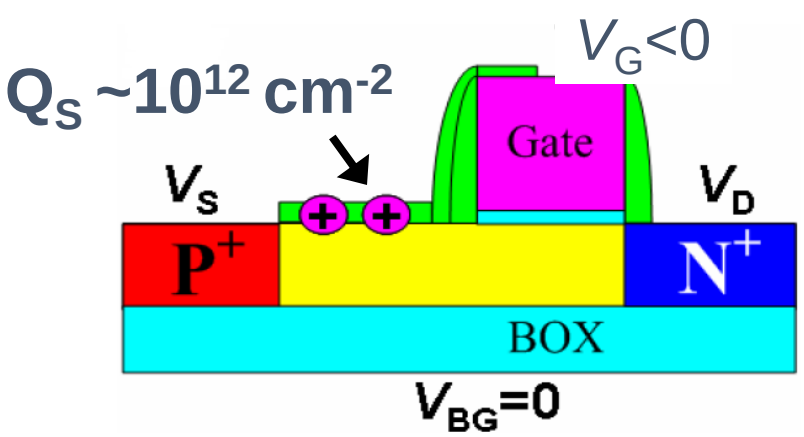


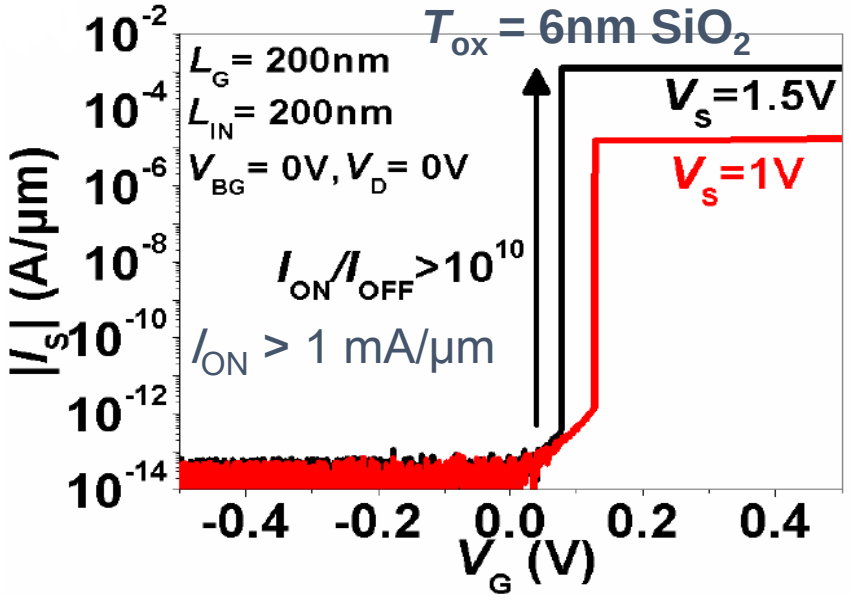


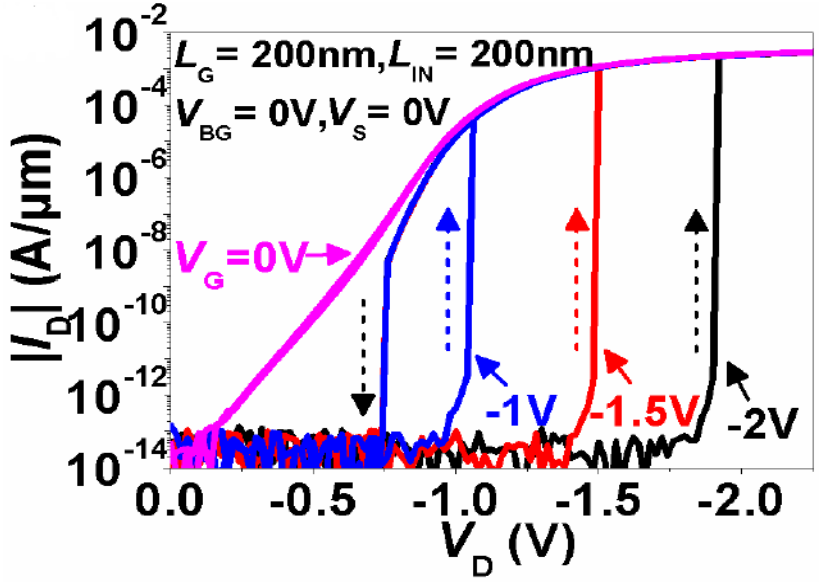
Z²-FET advantages: [Solaro et al, 2013]

- Low leakage current (< 10 fA/µm)
- Adjustable V_{t1} with gate bias
- V_{t1} > 1.1 V for V_{Gf} = 1.5 V & V_{Gb} = - 2 V
- High discharge current I_{t2} = 5 mA/µm

Z²-FET with Surface Charge

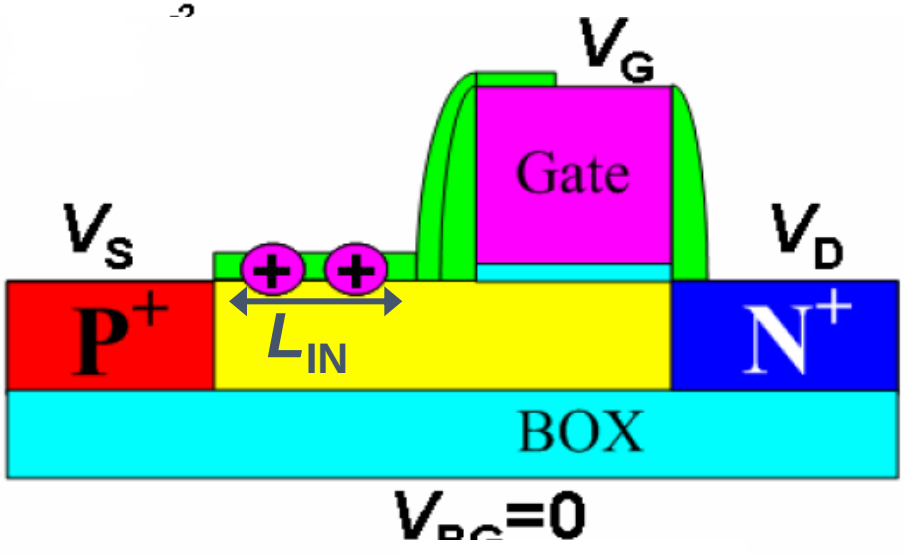


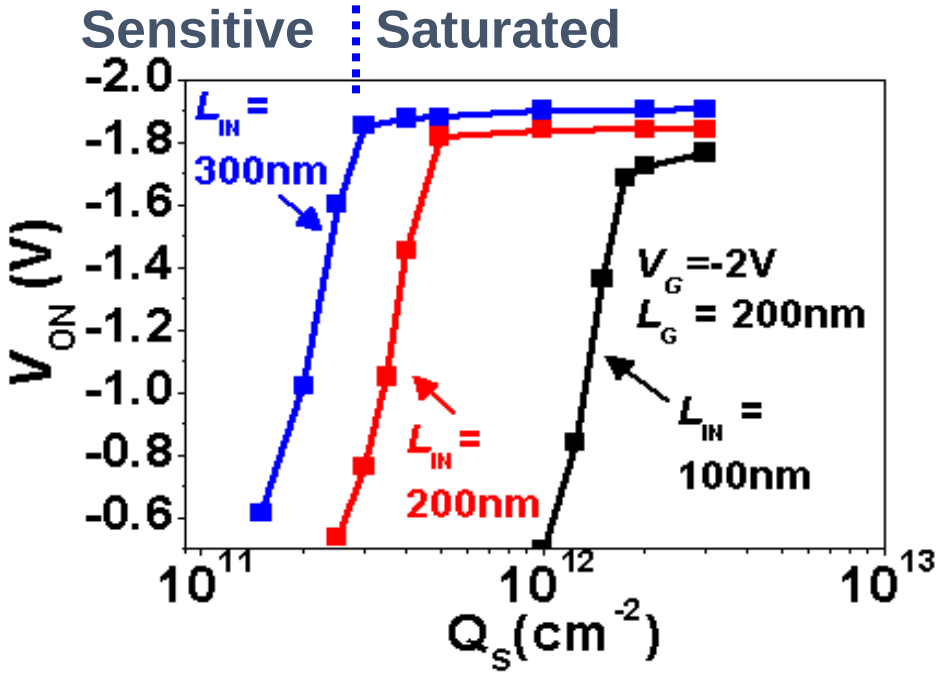




- Q_S replaces V_{BG} to create a barrier
- Similar sharp switching and V_G-controlled hysteresis as for V_{BG}-operated Z²-FET

Z²-FET: Charge Sensing





Z²-FET can be used as a bio-sensor

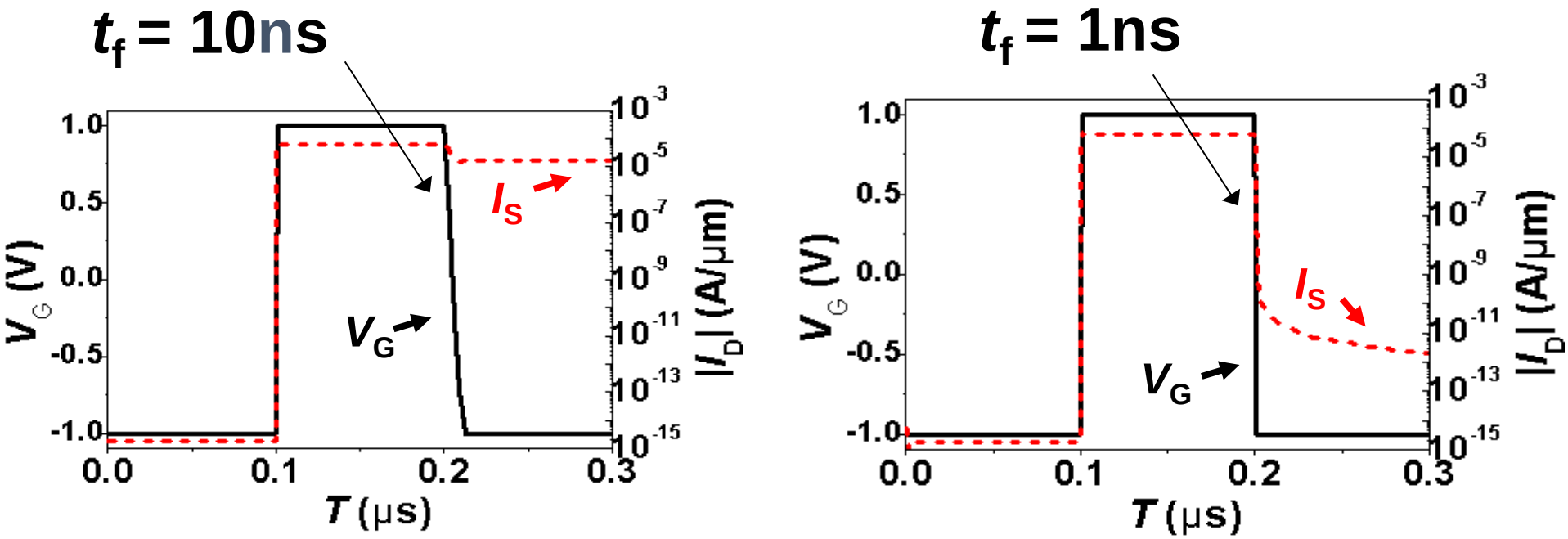
Surface charges can generate/modulate one barrier

High sensitivity of V_{ON} *vs* Q_S

Saturation occurs for large Q_S

L_{IN} modulates the sensitivity region: higher Q_S for shorter L_{IN}

Z²-FET Logic: Turn-off by Fast Pulse

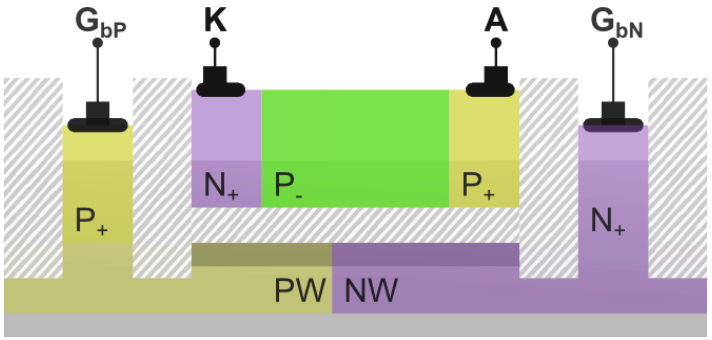


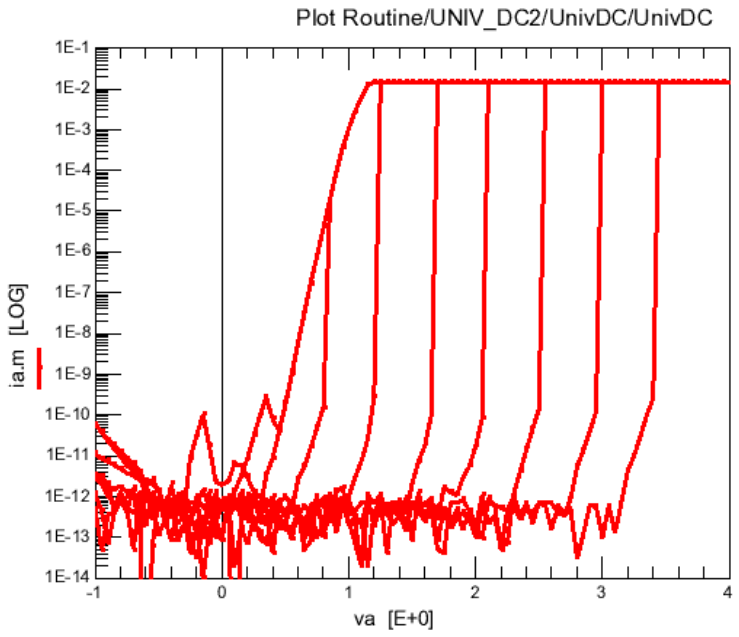
Simulations:

- V_G pulse with long fall time fails to turn off the device, agreeing with DC measurement
- V_G pulse with short fall time **can turn off** the device

  Similar to the mechanism in MOS-controlled thyristor [Huang et al., SSE 1993]

Z^3-FET Characteristics





V_{GbN} from 0 to 4 V and V_{GbP} = 0 V

Z^3 : Zero Gate, Zero Swing, Zero Ionization

or

Upside-down FED [Solaro et al 2014]

- Vertical $I_A(V_A)$ characteristics over 8 decades of current
- Low I_{OFF} & high I_{ON}
- No dielectric reliability issues
- Free surface: real estate available
  (pixels and ion sensors with sharp response)
- It comes for free with FDSOI
- Simplified CMOS process (no HKMG)

Conclusions

- Nano-size enables electrostatic devices with tunable doping level
- P-N junctions can be emulated or erased on demand
- Reconfigurable and versatile devices:

  breakdown voltage, reverse current, turn-on voltage, ideality factor, etc

- **Key question** – What is easier:
  - ion implantation?
  - gate fabrication?

- Sooner or later, the doping techniques will become inefficient and will be replaced by electrostatic doping

- Revolution in the architecture/fabrication of nano-devices …